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LOW COST INTEGRATED CIRCUIT TECHNIQUES

FINAL REPORT

BY

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PHILCO-FORD CORPORATION
Lansdale, Pennsylvania

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

1. PURPOSE

The purpose of this program was to develop batch processing techniques for passivating and completely terminating silicon integrated circuits to permit subsequent direct mounting and interconnecting of several circuits on a single substrate.

The work included the production of 50 preliminary exploratory development test models and their environmental testing according to MIL-STD-202 and comparison with similarly tested test modules assembled and mounted using standard integrated circuit procedures. This was done to demonstrate that the developed assembly and mounting techniques would not result in degradation of the devices. The tests also demonstrated the ability of chip coating to retain the high level of protection obtained from present hermetic packaging techniques. Also, the tests showed the ability of the flip-chip mounting technique to provide an increase in reliability over the currently used thermocompression bond.

In addition to the 50 individual test modules, four final exploratory development models were produced. These are arrays of three-input gate microcircuits, glass coated and interconnected as required by the contract.

2. ABSTRACT

An over-all process was developed for glass coating of silicon integrated circuit chips and batch attaching them to an appropriately processed substrate. The techniques developed were demonstrated by delivery of four 10-chip arrays consisting of glassed silicon microcircuits flip-chip assembled on a plug-in printed circuit board. Detailed information is provided concerning wafer glassing and other processing leading to flip-chip assembly.

In addition to the delivery of the final exploratory development models, other development units were fabricated and subjected to a test sequence intended to demonstrate the effectiveness of the developed process. Although the assignment of a quantitative failure rate was considered unrealistic because of the limited sample size, the analysis of the test data led to the conclusion that no catastrophic or major deleterious effects result from the combined glass and batch assembly process.

3. FACTUAL DATA

3.1 Introduction

The information in this section encompasses the entire period of program performance. However, the data and discussion related to work performed prior to the final quarterly period are restricted generally to presentation of highlights, whereas considerably more detail is included relative to the work performed in the final quarterly period.

The program was performed in the Lansdale, Pennsylvania facilities of the Microelectronics Division of Philco-Ford Corporation. Primary responsibility for performance of the program was assigned to the Materials and Process Development Department of the Microelectronics Division. The testing of the development modules in accordance with the test plan approved by USAECOM was performed by the Reliability and Control Department of the Microelectronics Division.

3.2 Completion of High-Temperature Preliminary Test Modules

At the conclusion of the fourth quarterly period, all the preliminary test modules had been constructed except those which were to be subjected to the 200°C storage tests. The Test Plan called for 15 modules to be subjected to the 200°C storage tests. The temperature involved in the tests required the use of a special printed circuit board and high temperature solder in the fabrication of the modules. During the early part of the fifth quarter, construction of these modules was completed. An additional 10 high temperature modules (for a total of 25) were submitted in order to have more information available.

Since the eutectic lead-tin solder melts at 183°C, the chips made with lead-tin solder pads could not be used for these tests. Pure tin will withstand the 200°C, but the increased solubility of nickel in tin required the process to be modified to permit the use of tin solder pads. Since a further change in the process was required because the standard G-10 epoxy printed circuit board will not withstand 200°C, it was necessary to select a separate printed circuit board and assembly process for the fabrication of the vehicles submitted to 200°C testing. For descriptive purposes, the modified process is referred to as the "high temperature" process.

It should be pointed out that the "low temperature" system utilizing G-10 epoxy board and lead-tin solder has sufficient

capability for practically all present electronic systems since they use printed circuit boards with temperature capability equal or inferior to the G-10 epoxy board. The principal need for the high temperature technique is therefore derived from its usefulness in accelerated testing of the microcircuit passivation.

The Third and Fourth Quarterly Progress Reports discussed in some detail the problems associated with wafer preparation caused by the increased solubility of nickel in tin. The Fourth Quarterly Progress Report also discussed the use of increased nickel thickness (about 25,000 Å) using Shipley Cuposit Electroless Nickel NL-61. This thickness was sufficient for use with tin solder. The wafer processing was otherwise identical to the low temperature wafer processing.

As previously mentioned, 200° C temperature prohibits the use of conventional G-10 epoxy board. In order to verify that the chips prepared with tin solder could be assembled, conventional epoxy boards were used for initial experiments. By adjusting the temperature, satisfactory flip-chip assemblies were made, thus giving confidence in the use of tin rather than the lower temperature lead-tin eutectic.

The two board materials which appeared to be most likely to perform satisfactorily at 200° C were a Teflon board and a silicone board. Since the laminating adhesive used with silicone board discolored after prolonged exposure to 200° C, the Teflon board was

initially selected, based on its higher temperature capability apart from its compatibility with the assembly process. Although, as mentioned above, the required number of modules were constructed, there are several factors which make the general purpose use of either of these boards less desirable than the G-10 board.

Briefly, most assembly difficulties were traceable to board softness and poor adhesion of the copper to the board. A major problem is movement of the narrow (5 mils) copper printed circuit pattern during the soldering operation which must utilize temperatures in excess of the 232°C melting point of tin. Soldering a chip onto the board at a temperature in excess of 232°C has a deleterious effect on the adhesion of the copper and causes the fingers to delaminate from the board. After soldering, the chip and the attached copper fingers are essentially floating. This condition has resulted in some broken solder joints.

Although the Teflon board has somewhat better bond strength (no adhesive is used, just a coating of FEP Teflon), the FEP Teflon used as a bonding agent does soften at the soldering temperatures. Excessive pressure on the copper fingers can then deform the bonding pads so that shorts may occur between the copper fingers and the silicon chips. Normally, the second step in the two-step soldering will raise the chip on "pillars" and eliminate any problems from this mechanism, but the deformation of the board

can be so great that the fingers are no longer sufficiently coplanar to insure that all bonds will remain. Assembly onto this board requires very close process control and the development performed was only adequate for fabrication of the required modules. The use of rigid printed circuit board (e.g., ceramic) would eliminate these problems and possibly result in a more satisfactory high temperature process.

Twenty-five modules were submitted for the 200°C storage tests. These modules utilized glass encapsulated chips. Only fifteen were required by the Test Plan, but additional modules were submitted to gain more confidence in the test results in view of the above mentioned difficulties associated with the high temperature modules. Controls assembled in TO-5 type enclosures were also submitted to the 200°C storage tests although no modules were flip-chip assembled utilizing chips without glass.

3.3 Final Exploratory Development Models

3.3.1 Description

As a demonstration of the processes developed during the contract period, four (4) integrated circuits, final exploratory development models, were constructed. These models each contain ten 3-input RTL gates encapsulated and assembled onto a single board. A photograph of the substrate used for the models is shown in Figure 1a. A schematic, consistent with the physical layout of the circuit, is given in Figure 1b. Note that common supply and ground leads are provided for the gates and all inputs are available at two edges of the board. It can be seen in Figure 1a that the common ground is accomplished by running a copper line under the chips. Figure 2 is a photomicrograph of the cross section of a portion of the final exploratory development model showing the location of the crossunder. A completed final exploratory development model is shown in Figure 3.

During the assembly of chips to the printed circuit boards it became apparent that if for some reason a bad chip is mounted, or a good chip is mounted incorrectly (misaligned with respect to the solder pads on the printed circuit board), the situation can be corrected simply by removing that chip and replacing it with another. This repair capability could be extremely important in construction of very large arrays, since the need for every chip

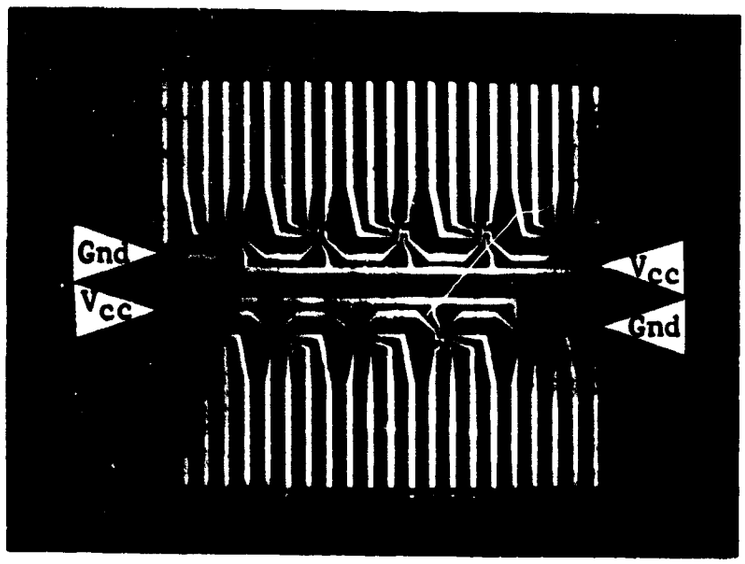


Figure 1a. Printed circuit board substrate for Final Exploratory Development Model.

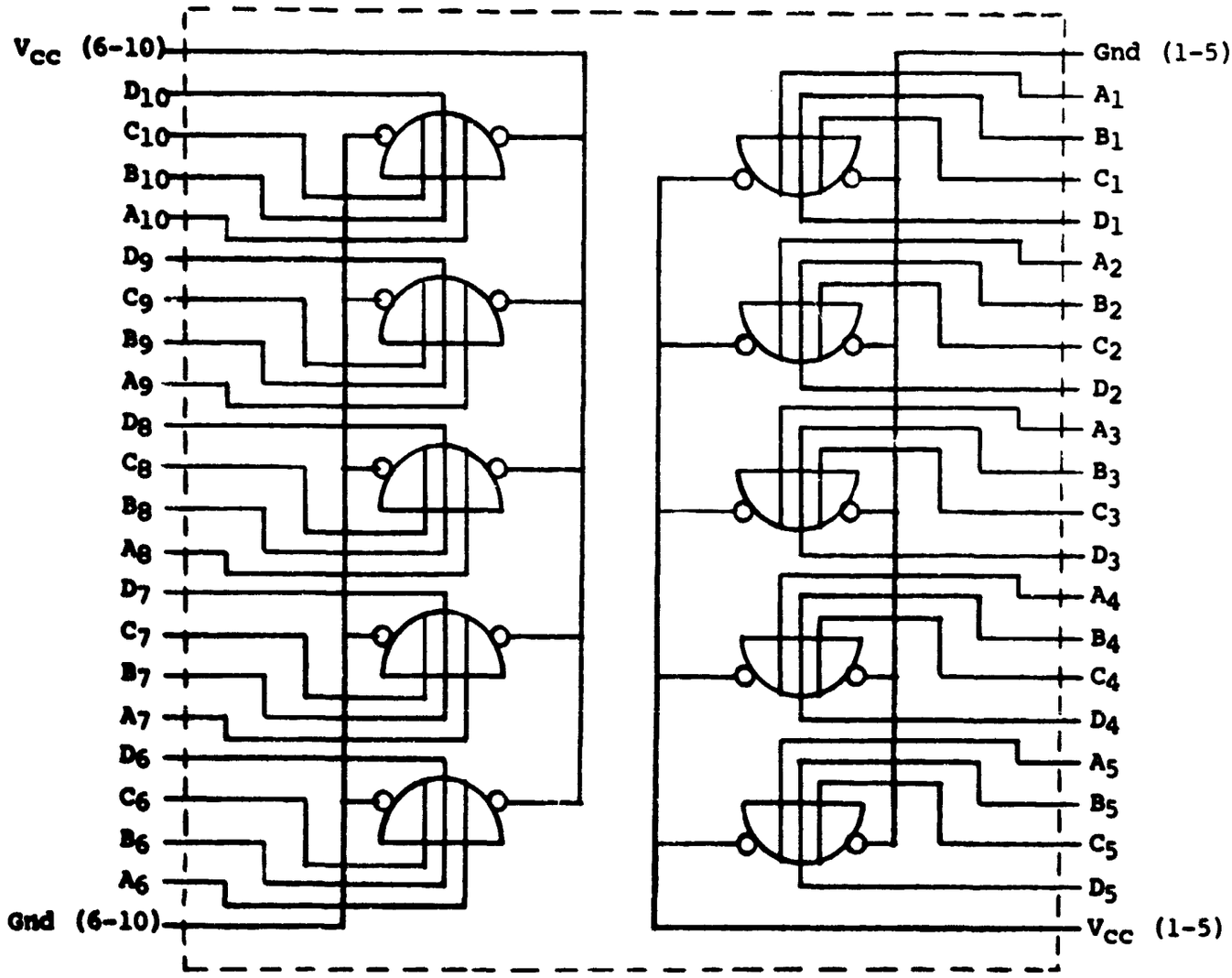
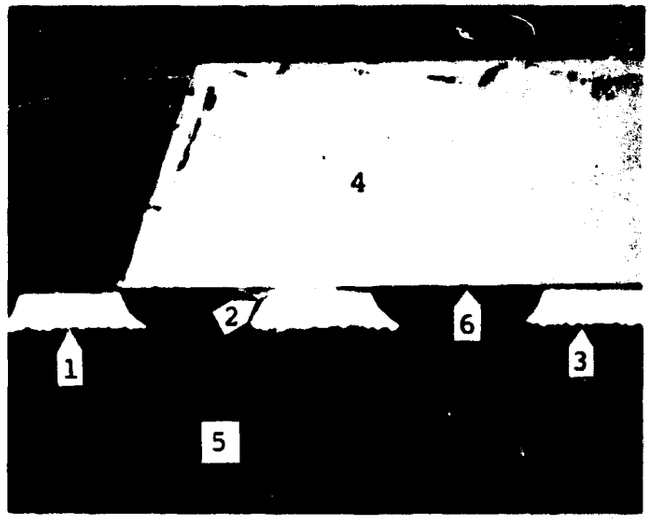


Figure 1b. Schematic diagram of Final Exploratory Development Model (array of ten 3-input gates).



LEGEND

1 - Alignment mark

2 - Bond to finger on printed circuit board

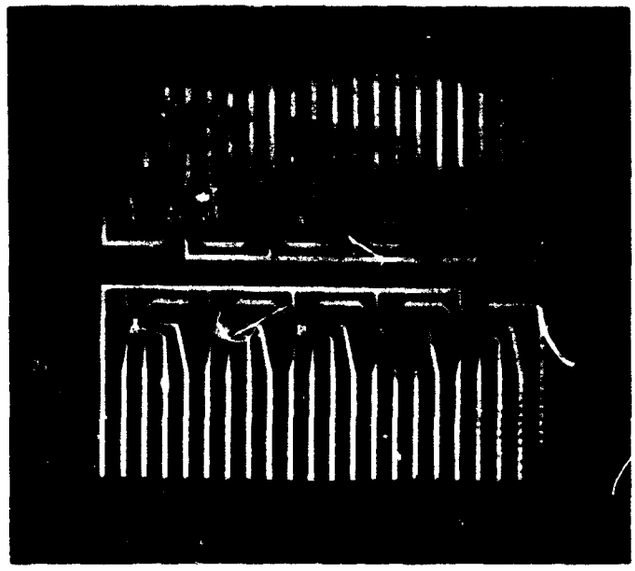
3 - Crossunder

4 - Silicon microcircuit chip

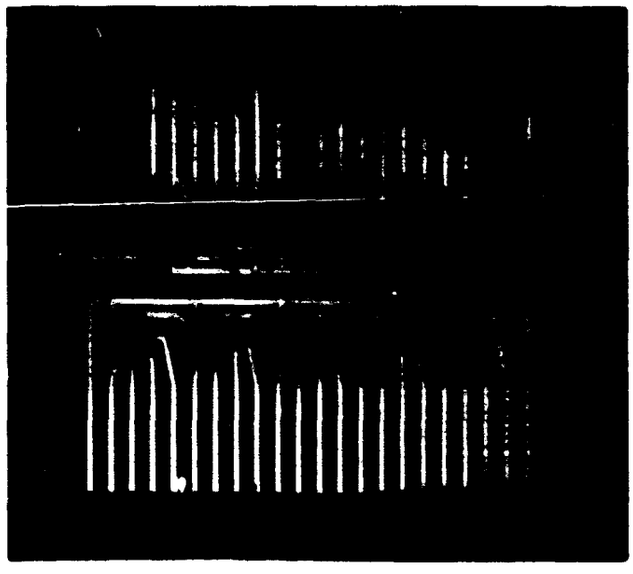
5 - Printed circuit board

6 - Glassed surface

Figure 2. Cross section of portion of Final Exploratory Development Model, illustrating crossunder.



a. Prior to application of epoxy protection.



b. Completed.

Figure 3. Final Exploratory Development Model.

to be guaranteed good is less pressing if it can be replaced without disturbing the rest of the assembly. Of course, this step must be carried out before the application of the epoxy coating used for mechanical protection of the assembled chips.

Figure 4 shows photographs of the three-input gate chip, without and with vapor plated glass, prepared for soldering to a printed circuit board. Figure 5 shows a photograph of a 10-chip array with all leads brought to one edge of the board, constructed during the fourth quarter of the program. Figure 5 also includes a preliminary test module.

3.3.2 Delivery

The required four final exploratory development models were delivered on 9 September 1966 at which time a conference was held at Ft. Monmouth, N. J. between representatives of USAECOM and the contractor. The models had been tested to meet the room temperature electrical specification for the PL-903 three-input RTL gate. The electrical parameter measurements of the individual integrated circuits were provided with the delivered models.

3.4 Materials and Batch Processing for Passivating and Completely Terminating Silicon Integrated Circuits

Of primary interest was the development of a glass deposition process compatible with a batch assembly process which would lead to a completely terminated integrated circuit. The following

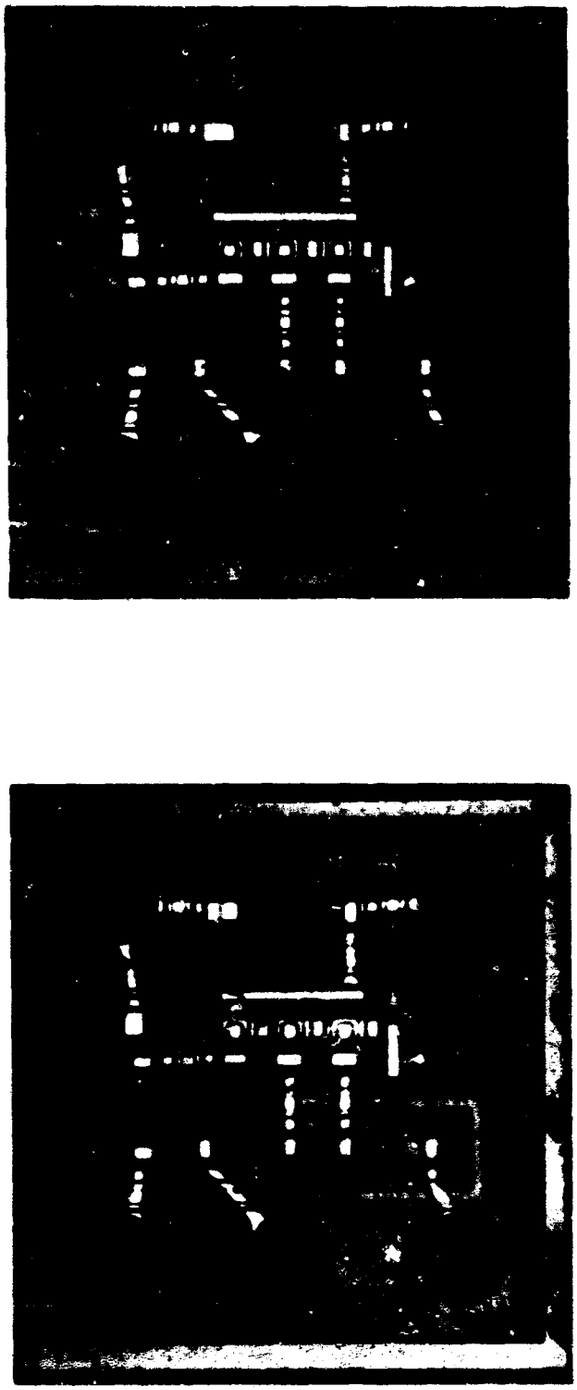


Figure 4. RTL gates with (top), and without (bottom), glass encapsulation.

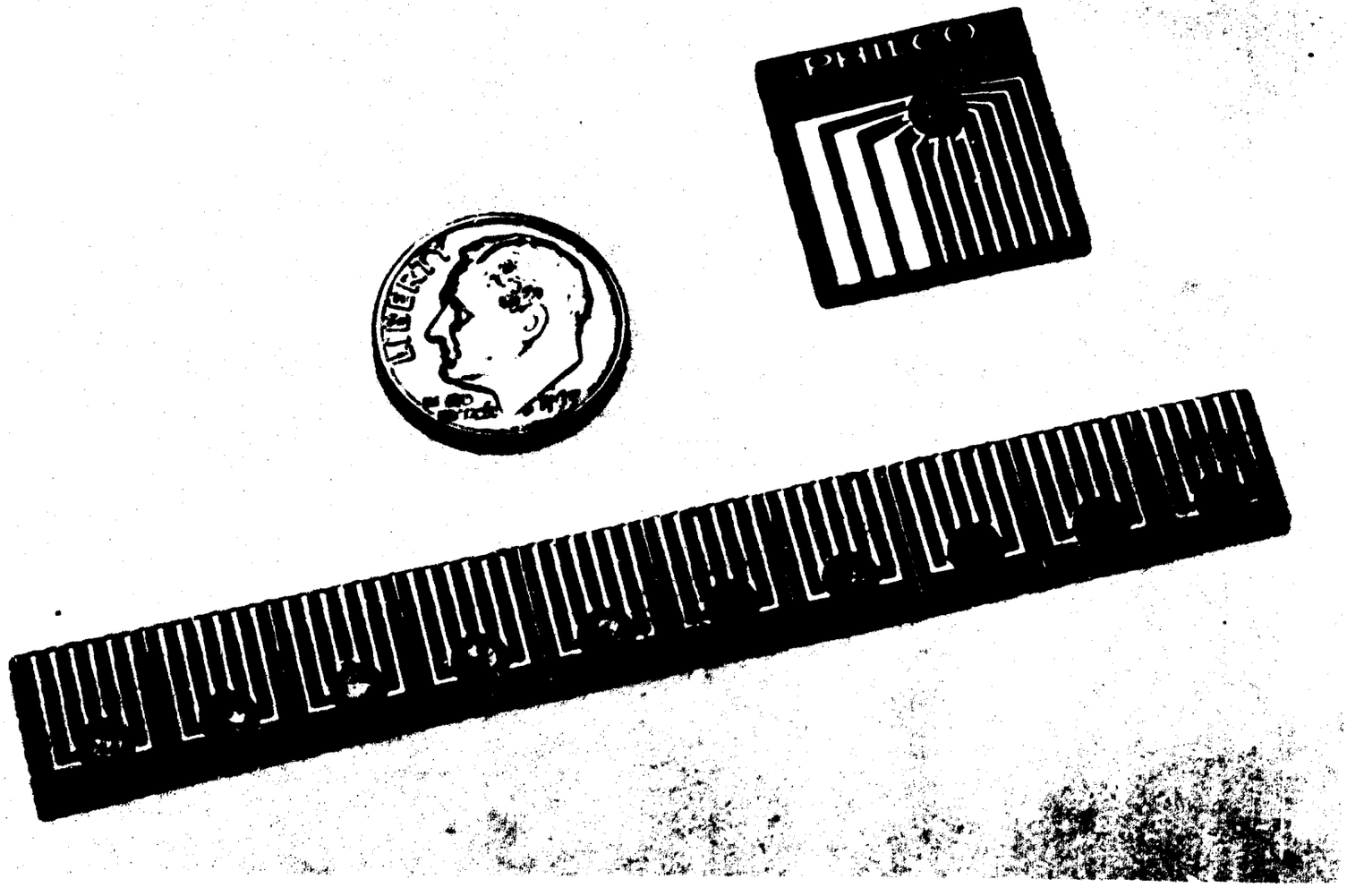


Figure 5. A 10-chip array of RTL gates.

paragraphs describe the glassing process as it was developed and finally used in preparation of the samples used on this program. The standard flip-chip batch assembly technique, although not developed under this program, was used in assembling the low temperature modules. In order to fabricate the high temperature modules, there was additional development work expended on this program to implement wafer processing changes which would permit the high temperature modules to be fabricated. Both wafer processes and the assembly technique are described.

3.4.1 Batch Glass Coating Process

Our initial approach to batch passivation was tungsten coil evaporation of Pyrex 7740 glass through metal masks onto the silicon wafer. Figure 6 is a photograph of a chip made with this technique. At the same time, other techniques for the deposition of glass films were being evaluated. By the third quarter of the program considerable data had been accumulated which indicated that vapor plated SiO_2 is better than evaporated glass in many respects. In particular, the vapor plated SiO_2 is superior as follows:

1. Less mobile charge is present.
2. The standard microcircuit aluminum metalization can be retained (400°C vs. 600°C substrate temperature used in evaporation).

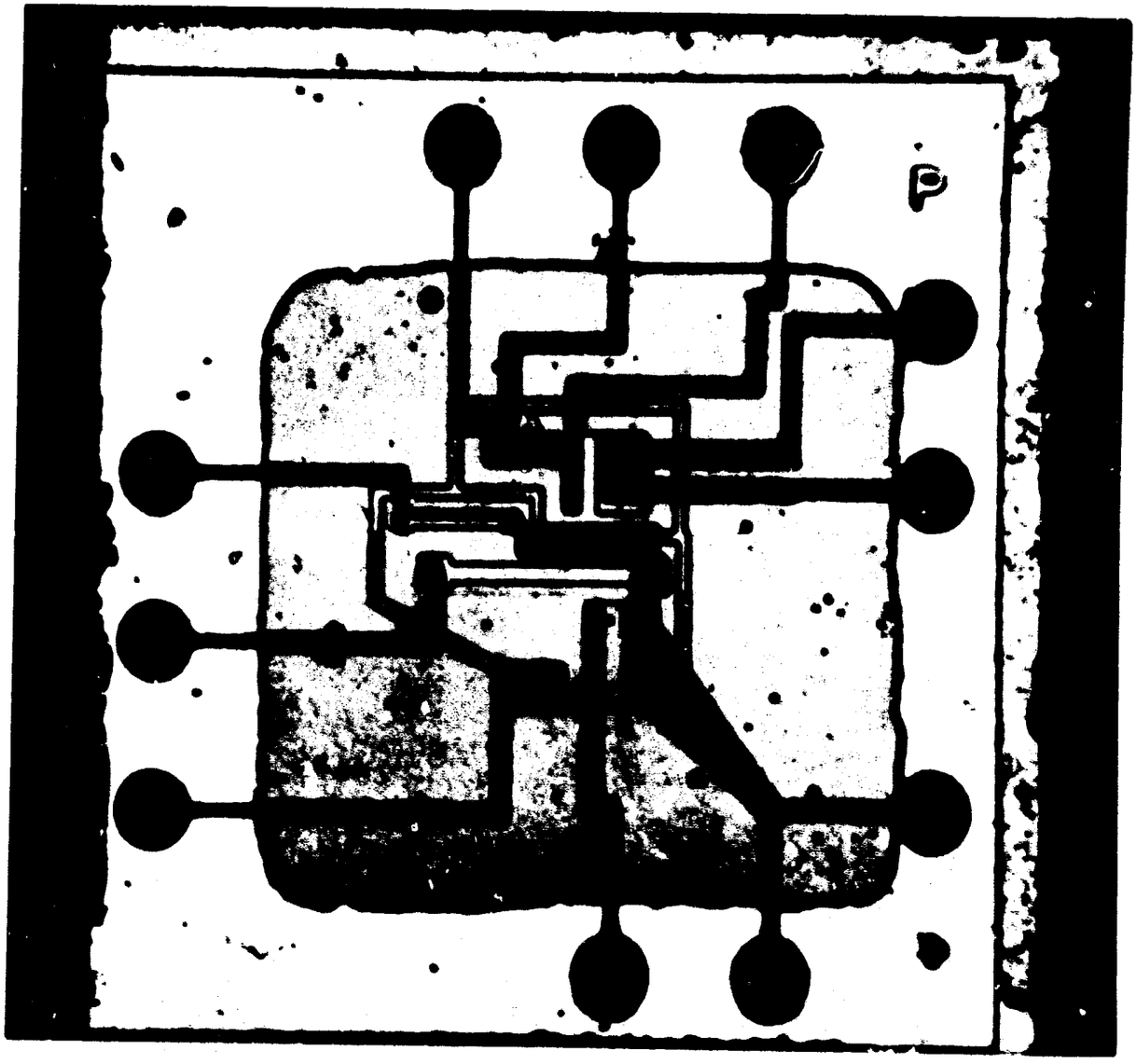


Figure 6. Silicon microcircuit chip encapsulated with evaporated glass.

3. Its dielectric properties are considerably better.

4. Better conformity to surface topology.

The First Quarterly Progress Report discussed the requirements of a glass passivating layer. The Third Quarterly Progress Report included a detailed comparison of the evaporated Pyrex glass and vapor plated SiO_2 passivating techniques. The Fourth Quarterly Progress Report presented data demonstrating the stability of device characteristics during the vapor plating operation.

After evaluation of oxides deposited by several vapor plating reactions as described in the First Quarterly Report, we selected the system described by the reaction

$$SiH_4 + 2O_2 \xrightarrow{\approx 400^\circ C} SiO_2 + 2H_2O.$$

This system was chosen because it gave evidence of performing better than others at temperatures near 400° C. Other contributing factors included speed of deposition, simplicity of control as a result of being a single component deposition, and ease of operation.

Vapor plating is a relatively simple procedure and is accomplished by placing the integrated circuit wafer on a heated substrate beneath a nozzle dispensing a mixture of SiH_4 diluted with dry N_2 and mixed with O_2. This mixture flows down onto the wafer where the hot surface causes the reaction to occur, depositing a film of SiO_2. The apparatus is shown in Figure 7 . The connection

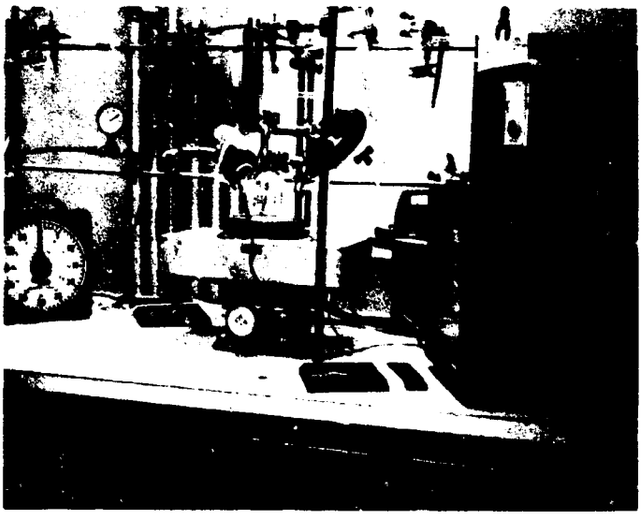


Figure 7. Two views of the SiO_2 vapor plating system.

scheme used for the various valves and flowmeters has not been found critical. It should be remembered that silane must be treated with adequate safety precautions and care taken to insure that no oxygen is present in the system prior to introducing the silane. The rate of deposition can be varied by changing the SiH_4 and N_2 ratios without seriously affecting the glass structure as measured by the glass etch rate. The etch rates for several gas ratios are shown in Table I.

TABLE I

Dependence of Plating Rate and Film Structure on Gas Flow Ratios

Dilute SiH_4 (From Tank) (cc/min)	N_2 (cc/min)	O_2 (cfh)	Plating Rate (Å/min)	Etch Rate (Tol. = ±5Å/sec)
500	5000	1	7600	150
500	7000	1	4500	143
600	5000	1	9400	153
600	7000	1	7000	150
700	5000	1	10000	153
700	7000	1	9300	153
800	5000	1	13250	160
800	7000	1	11200	146

Since the SiH_4 is diluted approximately 800:1 with N_2, the silane is now purchased partially diluted (3.6% silane in nitrogen has been used) to reduce the danger associated with its handling.

A nozzle diameter of approximately 3 cm is satisfactory for use in plating one wafer at a time. Nozzles up to 15 cm in diameter have been used for simultaneous plating of seven 1-1/4" diameter wafers.

Two techniques are available for obtaining desired thicknesses. First, rate of deposition being such that the plating time is on the order of minutes, one can measure the rate of plating for a particular set of conditions and then control the thickness by controlling the plating time. A more desirable technique utilizes a photometer which works on the principal of constructive and destructive interference of monochromatic light reflected from the plated oxide surface and light reflected from the wafer surface. The photometer method has proved to be very satisfactory in that it displays the deposition while it is occurring and, with the addition of a chart recorder, permits greater accuracy in achieving desired thickness control.

3.4.2 Wafer Processing

3.4.2.1 Standard Solder Process

Evaporation of Pyrex glass from a tungsten coil requires a substrate temperature of 600° which in turn requires a metalization system capable of withstanding higher temperatures than are withstood by the aluminum-silicon system. Although a number of systems are available for temperatures in the 600°C range, titanium-silver-titanium was used initially. The vapor plating

process will deposit satisfactory "glass" at temperatures below 400° C. Therefore, an encapsulation process which retained the aluminum metalization was developed. The Third and Fourth Quarterly Reports discussed the evolution of the present process which is summarized below:

The microcircuit wafer is fabricated in the conventional manner through metalization. A layer of solderable metal is then applied to the bonding pads. Next, the wafer is vapor plated with glass. The bonding pads are then exposed by etch-back techniques. The wafer fabrication is completed by dipping it into a solder bath to form solder pads.

The principle areas of effort in making the above process workable, other than optimizing the vapor plating process itself, were the delineation of contact holes through the glass, and the protection of the aluminum from attack during the application of the layer of solderable metal to the bonding pads.

Since the vapor plating process does not readily lend itself to close tolerance delineation by deposition through metal masks, a delineation process utilizing etch-back techniques was developed. If the glass were to be utilized as a dielectric in multilevel metalization for integrated circuits, it would be necessary to use the etch-back process to meet the tolerance requirements. Our results have shown that the selective removal of the vapor plated

SiO_2 from aluminum is not difficult, although care must be exercised in the design of the etch-back pattern to insure that the etchant used to remove the vapor plated SiO_2 never reaches the very-easily-etched phosphorus glass formed on the surface of the wafer during the emitter diffusion and which is necessary for device parameter stability.

Two techniques are available for protecting the aluminum from attack during electroless nickel (the solderable metal) plating. One technique uses a film of evaporated chromium and nickel applied before plating, and depends on the aluminum having a smoothness sufficient to make the film act as a barrier to the plating solution. The other technique also uses evaporated metal but utilizes plating solution that does not attack the aluminum. The first technique (a standard process available at the time) was used in constructing the low-temperature test models; the second was used for the high-temperature test models.

The low temperature process is outlined in detail below:

1. Fabricate the wafer by standard microcircuit processing through aluminum delineation.
2. Apply a photoresist mask which leaves the bonding pads exposed. This mask is used as a rejection mask for the chromium and nickel. Rejection is used because it is considered impractical to selectively etch chromium from aluminum.

3. Clean-up etch the aluminum to remove traces of oxide or other impurities. A dilute solution of KOH may be used.

4. Evaporate chromium onto the wafer to a thickness of 700 Å, followed immediately with nickel to a thickness of 1500 Å. The evaporations are done without the use of substrate heat.

5. Remove the rejection mask (thereby removing the Cr-Ni from everywhere but the bonding pads). This is accomplished by first soaking the wafer in warm trichloroethylene for a few minutes, followed by a gentle swabbing of the wafer. The wafer is then subjected to the normal photoresist removal process.

6. Apply photoresist mask for electroless nickel plating. This mask delineates the electroless nickel and prevents the plating bath from attacking the aluminum.

7. Electroless nickel plate with 6000 Å of nickel. A Philco-Ford proprietary bath has been used, but any of the commercially available baths of the alkaline variety would suffice.

8. Remove the photoresist.

9. Vapor plate with 15,000 to 18,000 Å of SiO_2 as described in paragraph 4.4.1.

10. Apply mask and etch the glass from the scribe lines. Buffered HF may be used.

11. Remove the photoresist.
12. Apply photoresist mask and etch the glass from the bonding pads. (If both areas were on one mask, steps 10 and 12 could be combined into one step). Again, a buffered HF solution may be used. Do not remove the mask.
13. Coat back of wafer with photoresist. Since most digital microcircuits have gold diffused into the wafer from the back, this step is necessary to prevent tinning the back of the wafer, which would make scribing and breaking difficult.
14. Tin the bonding pads by dipping the wafer in a water soluble flux followed by a 5-second dip in 60/40 solder at about 235°C. Immediately rinse in running deionized water to remove flux residue.
15. Remove the photoresist.
16. Die sort the wafer.
17. Scribe and break the wafer.
18. Bond the chips face down to printed circuit boards, using the soldering techniques described in paragraph 3.4.3.

3.4.2.2 Tin Solder Process

For reasons discussed in subsection 3.2, the models subjected to the 200°C storage tests required different processing. The major differences were the use of tin solder, which necessitated

a thicker film of electroless nickel, and assembly onto Teflon printed circuit boards.

The wafer processing described in the preceding section is valid except for steps 7 and 14 which, for the tin solder process, are:

7. Electroless nickel plate with about 25,000 Å of electroless nickel. (Shipley Cuposit Electroless Nickel NL-61 may be used.)

14. Tin the bonding pads by dipping the wafer in a water soluble flux, followed by a 5-second dip in tin solder at about 280°C. Immediately rinse in running deionized water to remove flux residue.

Obviously, the assembly of the chip onto the board requires a higher temperature to reflow the tin solder and, as discussed in subsection 3.2, a closer control on the bonding parameters to avoid excessive deformation of the soft Teflon board.

3.4.3 Individual Mounting of Chips to Substrate

The flip-chip assembly process as used on this program was developed entirely on company-sponsored activities.

After completing the additional wafer processing necessary to provide tinned contact pads on the microcircuit in wafer form, the process continues with conventional die sorting, scribing and breaking, and visual inspection. The microcircuit chips are placed face down

on a mirrored glass surface which is subsequently placed into the assembly machine. With the aid of a microscope, the operator orients the chip while viewing its surface in the mirror, and picks up the chip using a vacuum probe. The printed circuit board with its associated pad array and alignment marks are brought into the field of view beneath the chip (see Figure 8). Since the operator is viewing the chip at approximately a 40° angle with the horizontal, the original scribed edge of the chip is clearly visible. As the chip is brought in near contact with the pad array on the printed circuit board, the chip is positioned with the alignment marks. Rotation is achieved through the table supporting the board. Positioning of the chip in the x and y directions is accomplished through the micromanipulator to which the vacuum pickup is attached.

After the chip-to-board alignment is made and the chip put into contact with the substrate, the initial soldering cycle is activated. Heat is transmitted through the vacuum probe from a small resistance heater wound around the probe. A thermocouple embedded in the heater permits temperature control. Through judicious selection of time, temperature, and pressure, simultaneous solder joints are made between the two parts. To restrict the solder flow to the pad area, a temperature gradient is provided by cooling the copper pattern beyond the chip with a flow of nitrogen. Selection of force is a function of the pad area; a force of ~50 grams was used for the units assembled on this program. The assembly operation does not require flux.

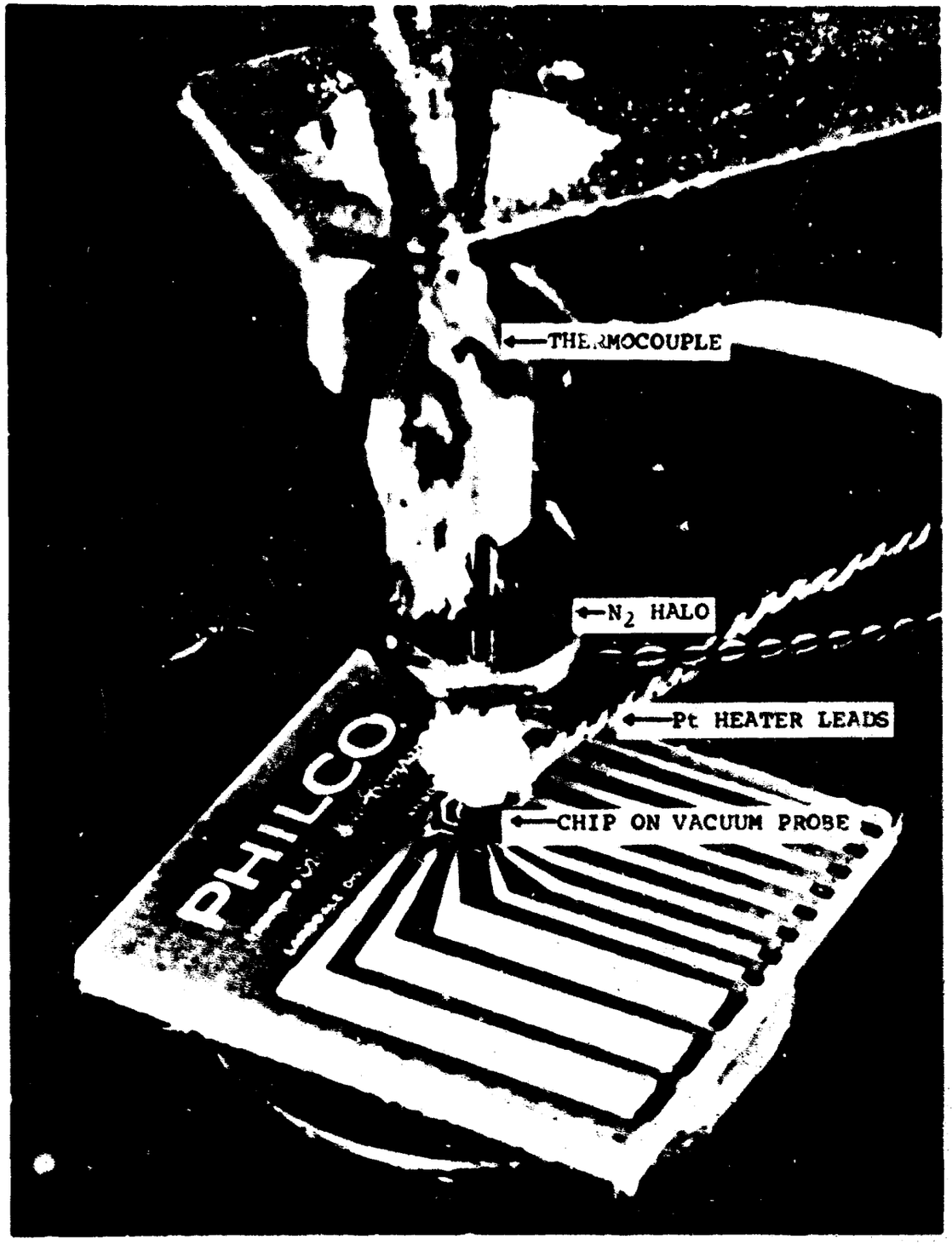


Figure 4. Flip-chip soldering fixture.

The second phase of the attachment process is accomplished by bringing the chip and board assembly beneath an infrared lamp source. A short heating cycle is provided to permit it to "float" on the solder joints, relieve the stress, and insure a space between the chip and the substrate.

3.5 Module Testing

Testing of the modules and an analysis of the test data were performed independently by the contractor's Reliability and Quality Control Department. The nature of the test vehicles, an outline of the tests performed, and a summary of the test results are given below. The detailed analysis of the test results made by the R&QC Department are included as an Appendix to this report. A commentary on the R&QC analysis is given in paragraph 3.5.5 from the device processing viewpoint, together with additional data that is considered useful in interpreting the test results.

3.5.1 Construction of Test Modules

The test modules used monolithic silicon devices containing:

a. A 0.5 mil geometry transistor,

b. A 1.0 mil geometry transistor,

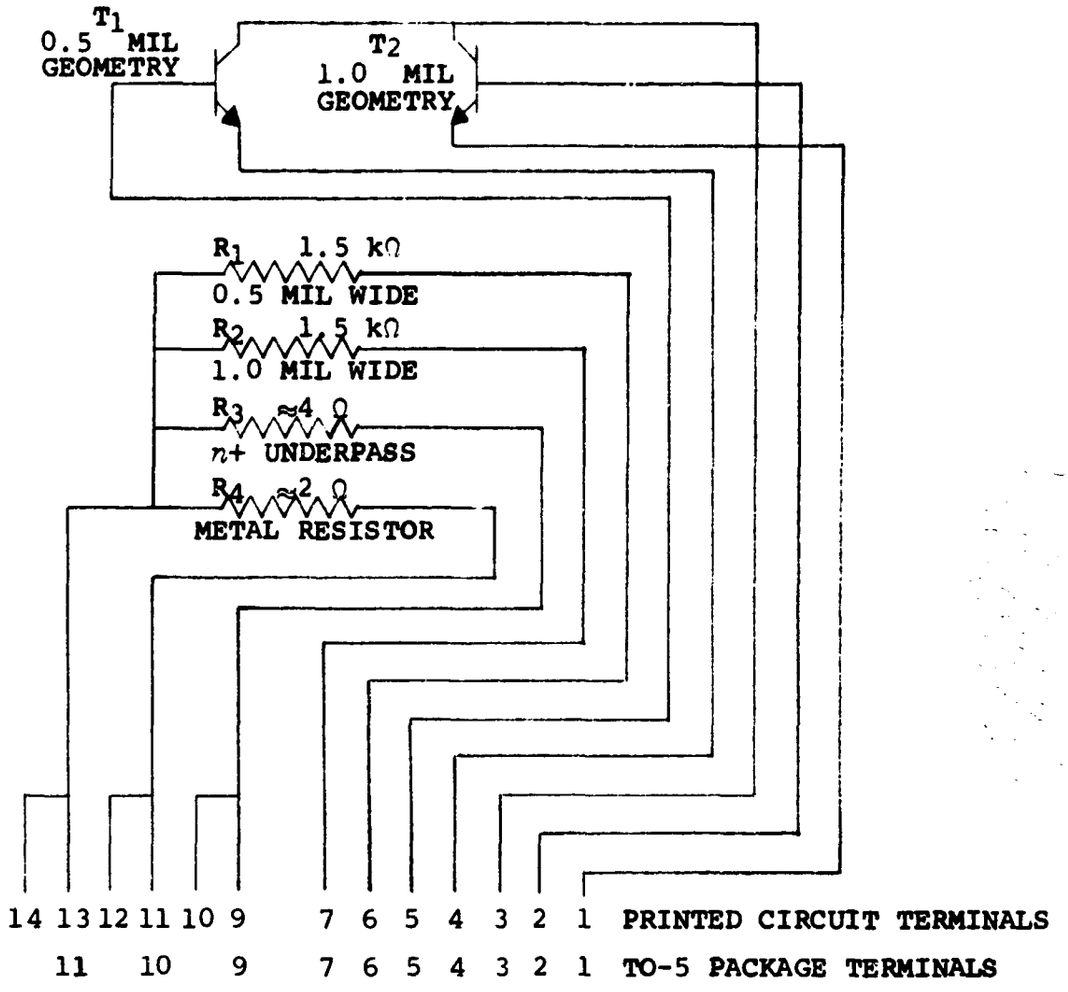
c. A 1.5 kΩ resistor of 0.5 mil width,

d. A 1.5 kΩ resistor of 1.0 mil width,

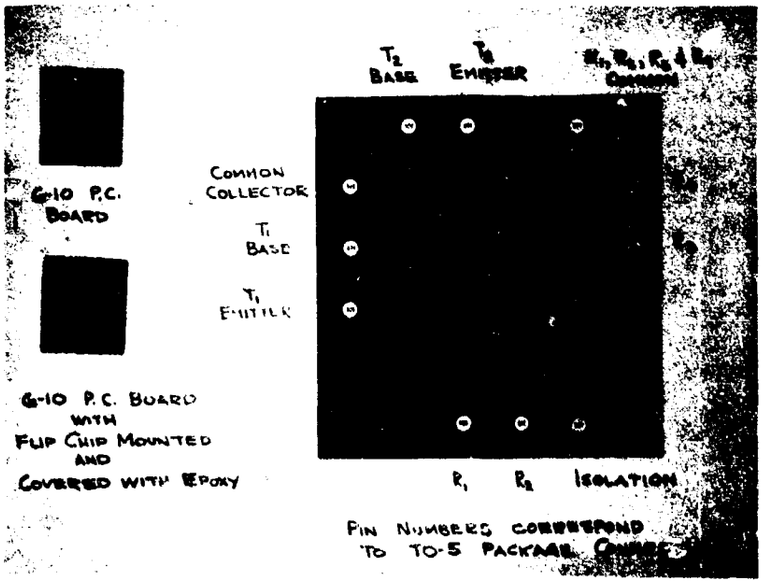
e. An n^+ underpass of approximately 4 Ω resistance,

f. A low value metal resistor, ≈ 2 Ω.

Terminations were made so that all components could be measured independently. Figure 9a is the schematic diagram of the test module A photograph of a test module with circuit connections identified is shown in Figure 9b.



a. Schematic diagram.



b. Photograph.

Figure 9. Test module.

The monolithic silicon devices were assembled as follows:

a. Sixty-two (62) were encapsulated in TO-5 packages. These devices, used as controls, were fabricated according to normal processing techniques, including gold nail-head bonding.

b. Twenty (20) were flip-chip assembled on G-10 material printed circuit boards that were etched to obtain an interconnection pattern conforming with the bonding pads in the device mounting area and terminated to conform to a standard printed circuit connector. The surface of these devices was passivated only with normal thermally grown oxide. The devices were attached to the printed circuit boards with lead-tin solder and covered with epoxy. These devices were subjected to environmental and 125° reverse bias testing.

c. Fifty-seven (57) were given an additional surface passivation by vapor plating glass over the thermally grown oxide, were also flip-chip assembled as indicated in b above, and subjected to environmental and 125° reverse bias testing.

d. Twenty-five (25) were given an additional surface passivation by vapor plating glass over the normal thermally grown oxide and flip-chip assembled onto Teflon printed circuit boards etched in the same geometry as described in b above. These devices were attached to the printed circuit boards with high temperature solder and covered with epoxy. They were subjected to 200°C storage life testing.

3.5.2 Test Plan

3.5.2.1 Environmental Testing

Thirty (20) TO-5 encapsulated devices, eleven (11) unglassed flip-chip devices, and twenty-three (23) glassed flip-chip devices were subjected to the following environmental test sequence.

1. Thermal Shock, per MIL-STD-750, Method 1056.1, 0°C to 100°C, 5 minutes at each temperature extreme, immediate transfer.
2. Mechanical Shock, per MIL-STD-750, Method 2016.1, 1500 G, pulse duration 0.5 ms, five (5) blows in each of three (3) planes*.
3. Vibration, Variable Frequency, per MIL-STD-750, Method 2056, 20 G, four sweeps from 100 to 2000 to 100 cps in each of three (3) planes*.
4. Constant Acceleration, per MIL-STD-750, Method 2006, 20,000 G, three (3) planes*.
5. Moisture Resistance, per MIL-STD-750, Method 1021.1, except that initial conditioning was not performed.
6. Moisture Resistance, per MIL-STD-750, Method 1021.1, with bias applied as per Figure 10.

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*See sketch at bottom of Table II (page 35) for definition of planes.

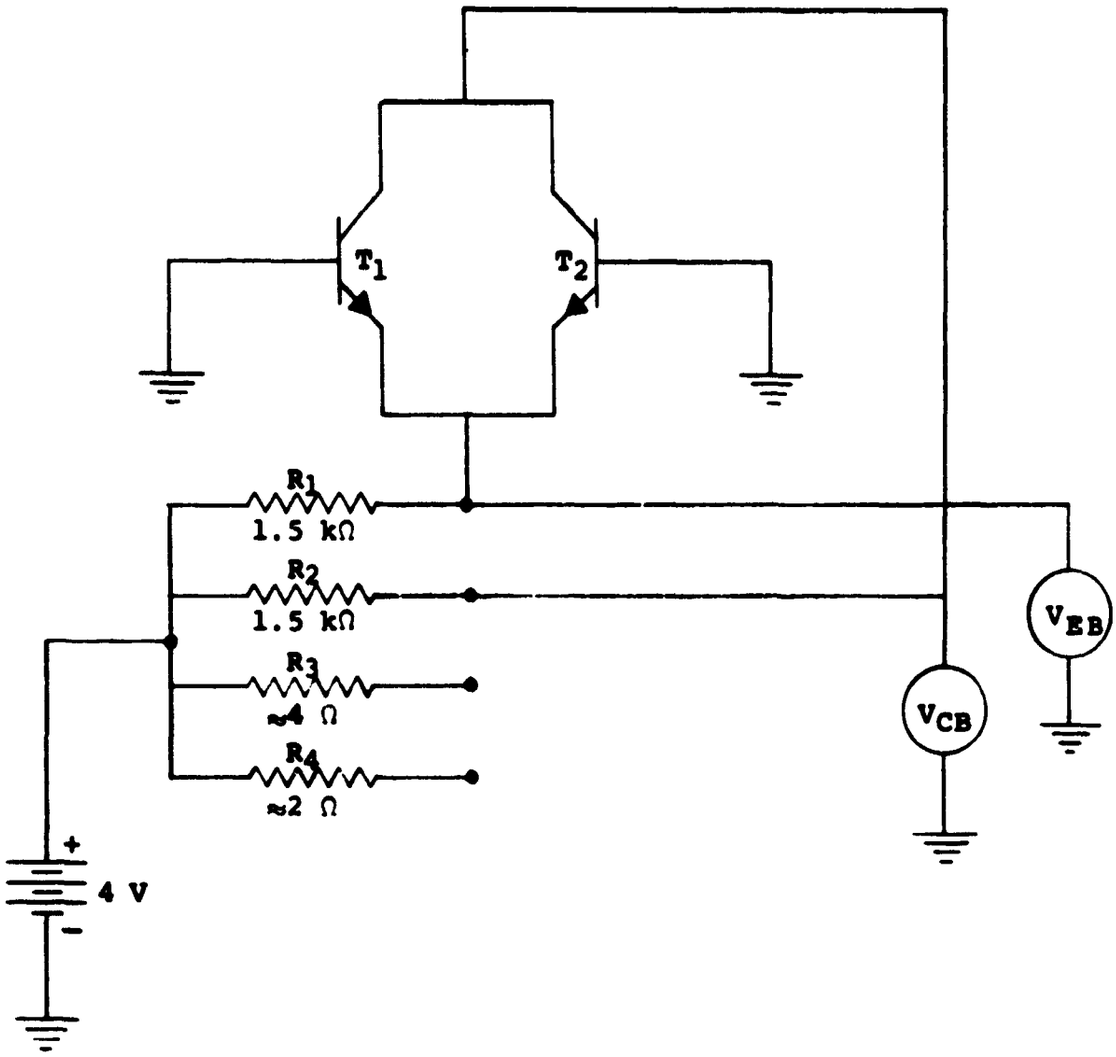


Figure 10. Reverse bias test circuit.

The test sequence was arranged in the above order to serve a multiple purpose:

a. To determine the capability of the devices to meet the normal MIL-STD-750 test requirements.

b. To determine if the thermal and mechanical stresses imposed during the test sequence would induce defects that would permit introduction of water during moisture resistance testing and cause subsequent failure during reverse bias testing because of electrolytic corrosion.

c. To compare the effects of this testing on devices fabricated with the unglassed flip-chip process and the TO-5 process.

At the completion of each environmental test, parameter measurements were made as specified in Table II.

3.5.2.2. Storage Life Testing at 200°C

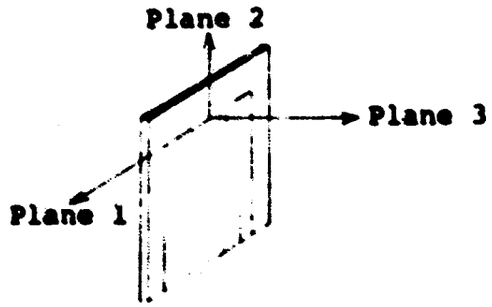
Twenty-five (25) modules made with glassed flip-chip devices and eighteen (18) TO-5 encapsulated devices were subjected to a 2000-hour, 200°C storage life test. Parameter measurements as specified in Table II were made at each reading period.

Because of the temperature requirements of this test, it was necessary to utilize a Teflon printed circuit board and high temperature solder for the fabrication of the test modules. There was some difficulty due to unsatisfactory adherence of the copper plating to the Teflon printed circuit board.

TABLE II

PARAMETER TEST CONDITIONS

ELEMENT	TEST	CONDITIONS
T_1 & T_2	I_{CBO}	V_{CB} = 5.0 V
T_1 & T_2	I_{CBO}	V_{CB} = 10.0 V
T_1 & T_2	I_{EBO}	V_{EB} = 4.0 V
T_1 & T_2	I_{EBO}	V_{EB} = 5.5 V
T_1 & T_2	BV_{CEO}	I_C = 5.0 mA
T_1 & T_2	h_{FE}	V_{CE} = 0.5 V, I_C = 50 μA
T_1 & T_2	h_{FE}	V_{CE} = 1.0 V, I_C = 1.0 mA
T_1 & T_2	h_{fe}	V_{CE} = 1.0 V, I_C = 1.0 mA, f = 1.0 kHz
T_1 (only)	V_{CE}(SAT)	I_C = 0.5 mA, I_B = 0.05 mA
T_2 (only)	V_{CE}(SAT)	I_C = 5.0 mA, I_B = 0.5 mA
T_1 & T_2	V_{BE}	I_C = 50 μA, I_C = 10 μA
T_1 & T_2	V_{EBF}	I_E (FORWARD) = 10 mA
R_1	Resistance	I = 1 mA, common lead pos.
R_2	Resistance	I = 1 mA, common lead pos.
R_3	Resistance	I = 10 mA, common lead pos.
R_4	Resistance	I = 10 mA, common lead pos.



ENVIRONMENTAL TEST PLANES FOR SHOCK, VIBRATION AND CONSTANT ACCELERATION

3.5.2.3 Reverse Bias Testing at 125°C

Nine (9) modules made with unglassed flip-chip devices, fourteen (14) modules made with glassed flip-chip devices, and fourteen (14) TO-5 encapsulated devices were subjected to this test. The intent of the test was to determine if the application of voltage at high temperature would induce polarization. The test circuit of Figure 10 was also used for this test.

All device parameters as indicated in Table II were read initially and after 2000 hours. At intermediate times only h_{FE} was measured. To preclude annealing of any polarization effects the devices were cooled to room temperature prior to removal of the bais at any of the reading periods. At the 2000-hour reading the h_{FE} measurements were made prior to any other parameter measurements.

3.5.3 Summary of Test Results

The failures which occurred during the environmental test sequence are summarized in Table III.

The results obtained in the storage life testing at 200°C are summarized in Table IV.

The results obtained in the reverse bias testing at 125°C are summarized in Table V.

3.5.4 Analysis of Test Results

The R & QC Department's analysis of the results of testing modules in accordance with the Test Plan outlined in paragraph 3.5.2 above is included in the Appendix to this report.

TABLE III

SUMMARY OF ENVIRONMENTAL TEST RESULTS

TEST NO.	FABRICATION TECHNIQUE	CUMULATIVE FAILURES							REMARKS
		SAMPLE	THERMAL SHOCK	MECHANICAL SHOCK	VIBRATION	CENTRIFUGE	MOISTURE RESISTANCE	MOISTURE RESISTANCE WITH BIAS	
L-1026	Unglassed Flip-Chip, G-10 Printed Circuit Board	11	0	0	0	0	9	11	All failures were catastrophic, due to electrolytic etching of metalization induced by introduction of water during the moisture resistance tests.
L-1028	Unglassed Chip, TO-5 Enclosure	30	0	0	0	0	1	0/15	Only 15 devices were subjected to the moisture resistance with bias test. One device showed a substantial change in V_{CE}.
L-1029	Glassed Flip-Chip, G-10 Printed Circuit Board	23	0	0	0	0	15	2/9	Of the 15 failures after moisture, 12 were catastrophic and 3 were V_{CE} degradation. There was a general increase in low value leakage currents after moisture resistance. Only 9 devices were subjected to moisture with bias testing and the 2 failures were catastrophic.

TABLE IV

SUMMARY OF 200° STORAGE LIFE TEST RESULTS

Test No.	Construction	Sample	Cumulative Failures 240 Hrs.	500 Hrs.	1000 Hrs.	2000 Hrs.	Remarks
L-2052	Glassed Flip-Chip, Teflon Printed Circuit Board	17	0	0	1	2	One open resistor at 1000 hours. One open resistor at 2000 hours.
L-2053	Glassed Flip-Chip, Teflon Printed Circuit Board	8	0	0	1	2	Both failures due to broken lead on printed circuit board.
L-2054	Unglassed Chip, TO-5 Enclosure	18	0	1	1	1	Degradation of resistor.

In addition to the above listed failures, 3 units could not be completely tested because of the delamination of copper from Teflon printed circuit boards.

TABLE V

SUMMARY OF 125° REVERSE BIAS TEST RESULTS

(Reverse bias of the collector and emitter = 4 V)

Test No.	Construction	Sample	CUMULATIVE FAILURES 168 Hrs.	340 Hrs.	440 Hrs.	670 Hrs.	1000 Hrs.	2000 Hrs.
L-4023	Unglassed Flip-Chip, G-10 Printed Circuit Board	9	-	0	-	0	0	0
L-4024	Unglassed Chip, TO-5 Enclosure	14	0	-	0	0	0	1
L-4027	Glassed Flip-Chip, G-10 Printed Circuit Board	14	-	0	-	0	0	0

REMARKS:
On all of the reverse bias tests, transistor T_1 indicated erratic readings during the h_{FE} measurement at V_{CE} = 1 V and I_C = 1 mA. These measurements were not consistent with the other data collected on this same transistor and were not considered for this summary. On Test L-4024, the single failure is an open resistor (R_3).

3.5.5 Discussion

3.5.5.1 Introduction

The following paragraphs discuss, from the device processing viewpoint, certain aspects of the results of module testing and analysis as given by the contractor's R & QC Department and reported in the preceding paragraphs of this subsection and in the Appendix. Also, additional data are presented to aid in the interpretation of the module tests.

Analysis of the test data demonstrates that the semiconductor device used in the modules survived the tests with no obvious failure mechanism; however, problems do exist in the protection of the metalization. The moisture resistance tests in particular are discussed in considerable detail and the failure mechanism is shown to be electrolytic corrosion of the metalization, a mechanism which can also affect TO-5 packages.

3.5.5.2 Parameter Grouping

Throughout most of the tests, the R & QC Department noted a tighter grouping of initial parameters on the TO-5 enclosed units than on the flip-chip modules. From the device processing viewpoint no significance is attached to this particular feature of the tests because:

A. Tests were run and reported in the Fourth Quarterly Progress Report, paragraph 4.3.2, which demonstrated that encapulsating with vapor plated glass causes no significant shift in parameters.

B. The tighter grouping of the TO-5 packaged units could be because all of them came from one lot, whereas the flip-chip units came from four lots. It was our original intent to select chips to be packaged in TO-5 enclosures from the same wafers from which the flip-chip units were selected. Accordingly, 145 TO-5 enclosed units and 325 test models were assembled from 6 lots. None of those TO-5 units were acceptable, although many test modules were. As discussed in the Fourth Quarterly Progress Report, paragraph 4.3.1, transistors which have been gold diffused to achieve low storage times will frequently have diode leakages in ex ss of 15 nA. For these tests we considered it necessary to select units with low leakage currents on the premise that a shift in this parameter would be a sensitive indicator in comparing the performance of glassed and unglassed units. Since these original TO-5 enclosed units were not acceptable an additional group had to be assembled and consequently these units did not come from the same wafers used to prepare the models. Therefore, the wider spread in parameters is not necessarily related to glassing.

3.5.5.3 Moisture Resistance Tests

Tests L-1026 and L-1029 indicate an undesirably high percentage of environmental failures during moisture resistance testing. The introduction of moisture can take place along the edge of the copper pattern which goes through the epoxy coating to the chip. As described in the following paragraphs, the glass coating can protect the chip from this moisture. Proper epoxy coating can also eliminate the source of moisture. The above mentioned test results are not consistent with tests performed on our company-sponsored programs. One of those modules utilized an unglassed flip-chip on a printed circuit board, test vehicle DP-2016, which involves the same chip used on the Final Exploratory Development Models (subsection 3.3). Ninety-seven DP-2016 vehicles were subjected to 10-day moisture resistance testing (R & QC Tests #L1003, L-1019, L-1021 and L-1033). Fifty of these vehicles had first been temperature cycled 20 times, +100°C to -65°C. Only one failure resulted. Moisture resistance data on unglassed chips have indicated that some assembly lots fail catastrophically while others completely pass. We have postulated that this lot to lot phenomenon is caused by improper handling of the epoxy used for the mechanical protection of flip-chip devices.

3.5.5.4 Electrolytic Corrosion

Every failed module which was taken apart evidenced open metalization. Considerable data have been gathered to show that the mechanism is electrolytic etching. (Consideration of the R & QC test data makes it apparent that the majority of failures occurred during measurement of electrical parameters).

This mechanism is also a problem of TC-5 enclosed devices, as discussed by Elkind and Hughes.* Generally, in situations which can lead to electrolytic corrosion, precautions are taken to prevent the accumulation of water. For example, in our moisture resistance test the TO-5 enclosed units are always tested with the package oriented to prevent water accumulating between leads. In systems applications, when TO-5 units are mounted onto printed circuit boards for use in high humidity environments, a conformal coating is provided to prevent water accumulation under the package.

To demonstrate how serious moisture accumulation can be, tests were performed to determine if a TO-5 lead could be etched to failure. New stems were obtained and the leads were twice bent to a 90° angle and then straightened. Then the packages were held upside down and water of various degrees of purity was dropped onto the stems with an eyedropper so as to accumulate

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* Elkind, M.J. and H.E. Hughes, "Preventing of Stress-Corrosion Failure in Iron-Nickel-Cobalt-Alloy Semiconductor-Device Leads", 1966 Physics of Failure in Electronics Symposium.

between the two leads to which voltage had been applied. The results were:

1. With 15 volts applied between the leads, and using a salt water solution, the positive lead fell off in less than 1 minute.
2. With 4 volts applied, and using a salt water solution, the positive lead fell off in 7¼ minutes.
3. With 4 volts applied, and using tap water, the positive lead fell off in 4½ hours.
4. With 4 volts applied, and using DI water, the positive lead fell off in 24 hours.

3.5.5.5 Analysis of Failed Modules

After extended exposure to high humidity environments, it was sometimes possible to remove the epoxy mechanical protection from the printed circuit board by inserting a razor edge at the epoxy-board interface. Often the chip was damaged in the removal process, but considerable insight into the failure mechanism was gained through this technique.

Figures 11, 12, 13, and 14 are photomicrographs of opened devices which had completed the moisture tests. The unclean appearance of the chips is due to traces of epoxy remaining on the chip surface.

The chip shown in Figure 11 failed because the collector metalization opened. This metal would be biased positive during

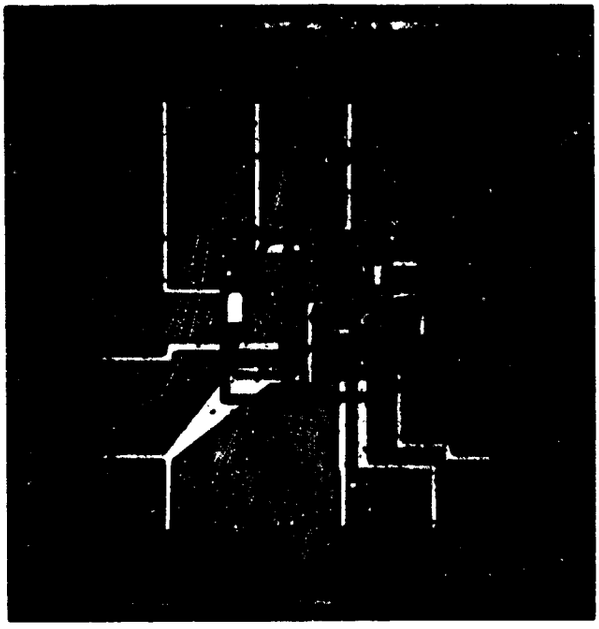


Figure 11. Test module chip, after removal from printed circuit board, showing electrolytic etching of metalization (see circled area).

Figure 12. Surface of the protective epoxy under the assembly showing the imprint of the chip shown in Figure 11.

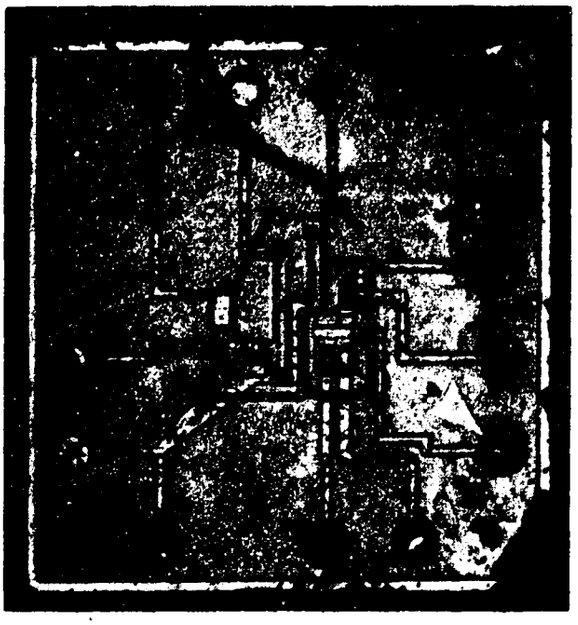


Figure 13. Test module chip, following removal from printed circuit board, also having electrolytic etching of collector pad as shown in magnified view in Figure 14.

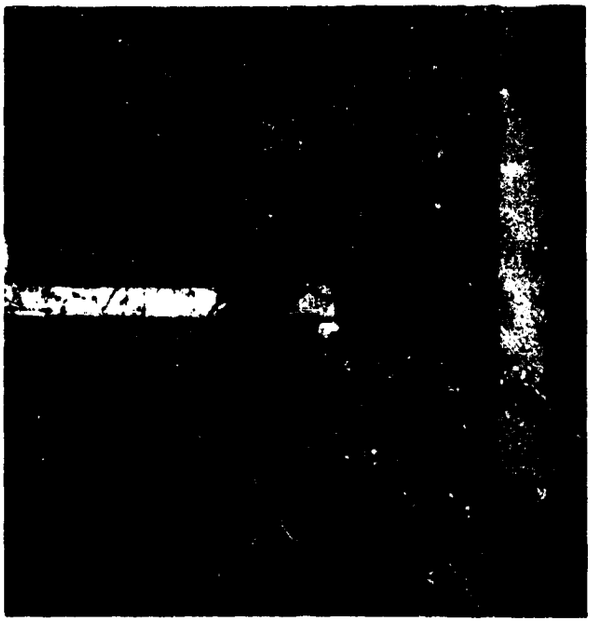


Figure 14. Magnified view of attacked metalization in region indicated by arrow in Figure 13.

testing. (In the etching of the TO-5 leads, it was always the positive lead which was attacked.) Figure 12 shows the imprint of the chip on the epoxy coating. The granular area corresponds to the air pocket formed under the chip by the epoxy flowing underneath the chip from all sides. It is also interesting to note that the location of open metalization on the chip does not correspond with the location of the air pocket. One might suspect that the air pocket area would be the area most likely to be troublesome because of the possibility of moisture being entrapped there.

Figure 13 shows another chip which failed at the collector metalization. In this case the failure occurred at the bonding pad which is shown in Figure 14. Since these modules were constructed at an early stage in the development of the vapor plating process, the control over etching the holes through to the pads occasionally allowed aluminum to be exposed beyond the electroless nickel. Since no effort was being made to protect the aluminum, these devices were acceptable at that time for use in the construction of the test modules. Close inspection of the bonding pads in Figure 13 reveals several defects in the glass close to other pads on the chip.

Figure 15 is a photomicrograph of a chip which survived the moisture tests. Note, in particular, the improved appearance of

the bonding pads in contrast with the appearance of the chips in Figures 11 and 13. The detail of a bonding pad is shown in the photomicrograph in Figure 16. Figure 17 shows the imprint of the chip shown in Figure 15 on the epoxy coating. The air bubble covers the greater part of the active area of the chip, implying that the location of the air bubble is not a factor in determining whether a chip survives or fails. (The scratch seen in the epoxy (Figure 17) was created during removal of the chip.)

Figure 18 is a photomicrograph of an unglassed chip otherwise similar to the chips used in the Final Exploratory Test Modules, which failed moisture tests after fifty days. The need for the protection afforded by a glass coating is obvious.

We believe that when the glass coats the aluminum properly, the units will not fail due to moisture. To test this theory, several chips which had passed the moisture tests were removed and immersed in an aluminum etchant for a sufficient time to remove the exposed aluminum. If the glass were acting as a barrier to the moisture, no attack on the metalization would be expected. If there were pinholes in the glass, obviously the aluminum would be dissolved. Since the positive lead or anode is the metal which is dissolved, the common collector lead would be a particularly good indicator. Figure 16 shows the collector metal on a chip,

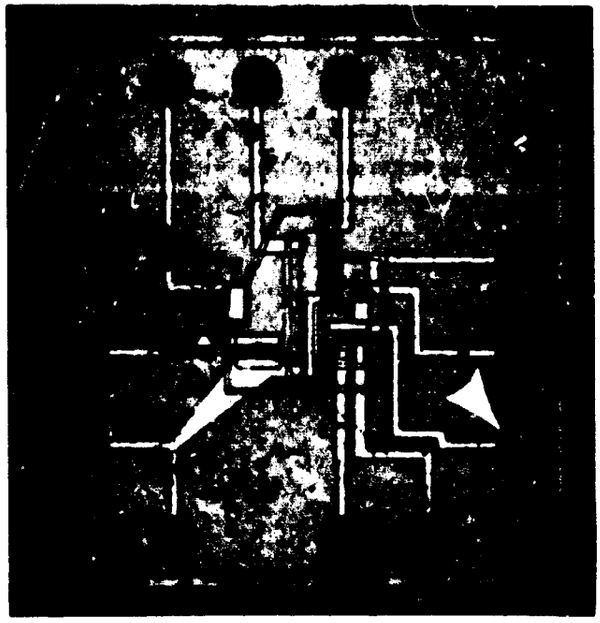


Figure 15. Test module chip after removal from printed circuit board. This chip had no evidence of electrolytic etching of the metalization. A magnified view of the collector pad is shown in Figure 16.

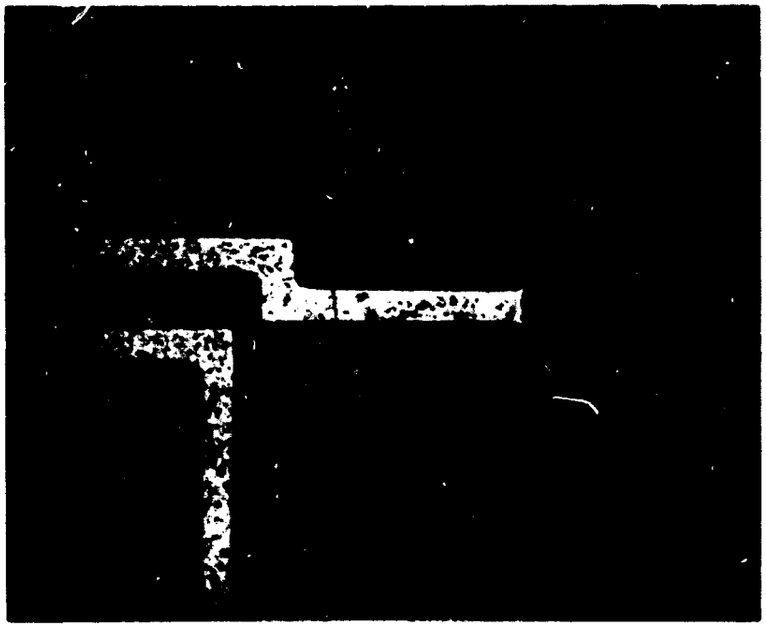


Figure 16. Magnified view of the collector pad of the test module chip shown in Figure 15. This view was taken after the chip was subjected to an aluminum etchant as described in the text (para. 3.5.5.5).

Figure 17. Surface of the protective epoxy under the assembly, showing the imprint of the chip shown in Figure 15.

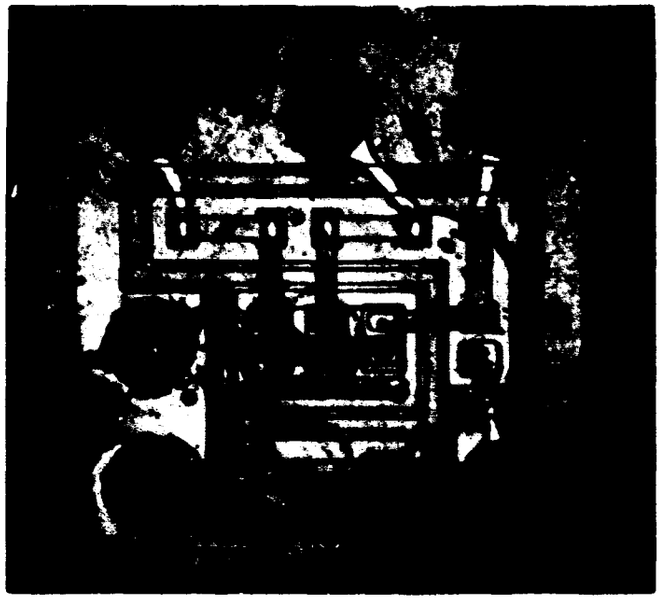


Figure 18. An unglassed chip after removal from printed circuit board. Electrolytic etching has removed nearly all the metalization from this chip.

which had passed moisture tests, after subjection to the aluminum etch. There is no evidence whatsoever of attack on the metal, even near the bonding pad. Similar results were obtained on other chips, implying that those units which survived moisture probably had better glass coatings insofar as metal protection is concerned. Figures 19 and 20 show for comparison an unglassed chip and a glassed chip before and after subjecting to an aluminum etchant. While an extreme example, the protection offered by the glass for the metal is clear.

Thus, it has been shown that if an objective of the glassing is to protect the aluminum metalization, such protection can be accomplished. We had not anticipated the requirement for this protection prior to the program. The initial unconcern for the metalization is obvious in Figure 6 (page 16), which is a photomicrograph of a chip passivated using the initial process of evaporating glass through a metal mask.

4.5.5.6 Resistor R_4

In order to measure the resistance associated with the termination process, resistor R_4, which is an aluminum conductor with a solder connection on each end, was included. Contact resistance values ranging from one to twenty ohms have been found on resistor R_4. Specific measurements of aluminum-pad resistance verified the presence of contact resistance which was traced to the interfaces of the chromium-aluminum and of the electroless

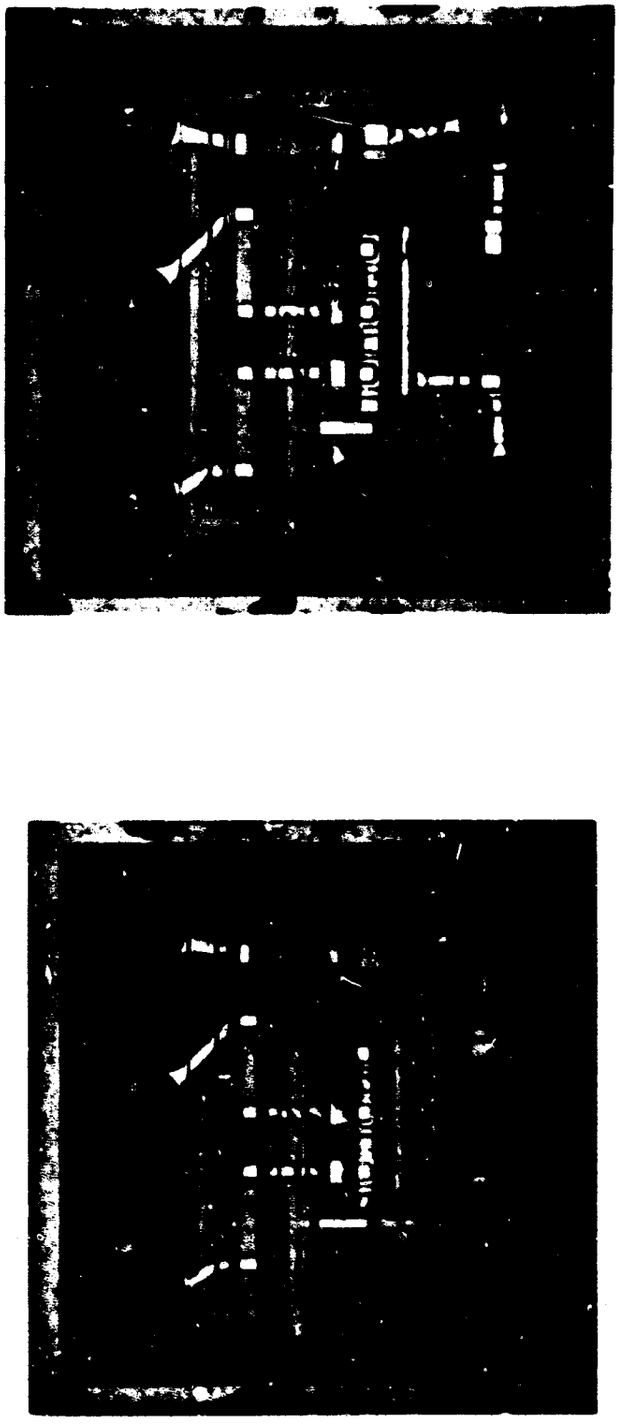


Figure 19. Device not protected by glass before (top), and after (bottom). 20 seconds in aluminum etchant.

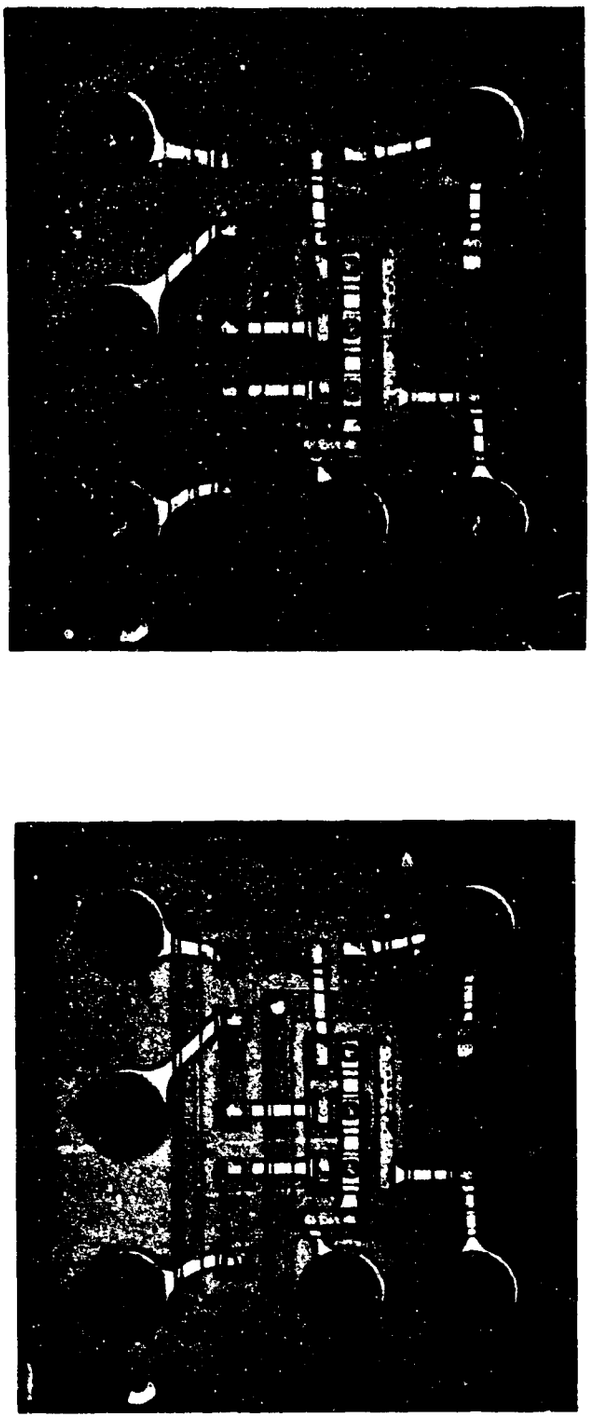


Figure 20. Device protected by vapor plated SiO_2 before (top), and after (bottom), 20 seconds in aluminum etchant.

nickel-evaporated nickel. More careful cleaning of the aluminum prior to fabrication, and careful control of the electroless nickel plating conditions have eliminated the problem. Current devices and prototype assemblies being fabricated with the process used in this program result in resistances between 5 and 15 milliohms per contact.

3.5.5.7 Summary

The objective of the passivation process was to provide a level of protection to the active areas of the semiconductor comparable to that offered by a TO-5 enclosure. The principal mechanisms for device degradation were expected to be surface charge build-up caused by fringing fields, or other sources of surface ions. Analysis of parameter shift during the test program demonstrates that the glassed devices are comparable to the devices encapsulated in TO-5 type enclosures. A problem which had not been anticipated was the protection required by the metalization. The number of catastrophic failures which occurred during moisture tests, although believed very pessimistic, demonstrates the need to protect the metalization as well as the semiconductor device itself. Auxiliary tests have shown that glassing can protect the metalization from attack.

4. CONCLUSIONS AND RECOMMENDATIONS

4.1 Conclusions

This program resulted in the development of a batch process for the deposition of a glass coating on an entire wafer of circuits. The coating protects the semiconductor from environmental conditions. The most serious evidence of the need for additional protection is the electrolytic etching of aluminum from the surface of the microcircuit which results from ionic contamination and the application of bias voltages.

Since the electrical stability of the microcircuit is largely dependent on the specific processing used by the individual manufacturer, it is required that the additional glass coating in no way degrade the device performance. Silicon microcircuits manufactured by the contractor were coated with glass deposited by the vapor plating process developed on the program. The device electrical parameters were unaffected by this glass coating. In fact, measurements made by MOS capacitance techniques showed the charge concentration of the vapor plated glass to be superior to that in other glass coatings that were investigated. Based on the work performed during the program, it is expected that the vapor deposited glass is compatible with most current manufacturing methods.

In conjunction with the flip-chip bonding process, which completely terminates the silicon integrated circuit and also

facilitates batch attachment, the compatible glassing technique results in an over-all assembly process as required by the contract. With specific attention to processing the glassed wafer so as to avoid the creation of pinholes which may expose aluminum, it was shown that complete protection can be afforded the microcircuit from environmental conditions. Although glass must not completely cover the termination metalization (i.e., the bonding pad material must be exposed), attack of aluminum in even these areas is limited by the chromium-nickel metalization.

One of the most valuable applications of the over-all glass and batch attachment process may be in the construction of multiple chip assemblies involving several integrated circuits connected on a single substrate. This use was demonstrated, as required by the contract, with printed circuit cards on which 10 three-input gate RTL circuits are flip-chip mounted. Supply voltage and ground leads are common to each of two groups of five circuits. The ground lead passes under the flip-chip circuits, further demonstrating the protection and design flexibility offered by the glass coating.

The glassed chip with its solderable pads is a complete circuit able to function without any further packaging. Connection to the next level of "system" wiring using the flip-chip approach is equivalent to attaching packaged devices to printed circuit

cards. The protected chip can be directly attached to and terminated on a wide variety of substrates. The size of the interconnection substrate is limited by the technology used in fabrication.

Although the relatively small number of units tested on this program does not realistically permit assigning a quantitative failure rate, it can be concluded that there are no catastrophic or major deleterious results from the combined glass and batch assembly process. Failures were encountered in moisture resistance tests; however, the cause has been determined and correction demonstrated. It is believed that the type of over-all assembly and packaging technique developed on the program can be significantly useful with silicon integrated circuits designed for achieving complex functions.

4.2 Recommendations

Additional investigations related to the completed program should be conducted in the areas of glass coating of microcircuit chips; batch attachment of chips to substrates; and reliability, both at the chip and system levels. A brief description of the nature of each of these recommended areas of investigation follows.

Although in the program just completed, the tangible benefit of glassing that was emphasized is the long term protection of the silicon chip from environmental contamination, consideration should

be given to the use of a hard glass coating for physical protection of silicon chips. A very serious problem in microcircuit device manufacture is that of scratching and deformation of the aluminum interconnection patterns during handling subsequent to wafer metalization. Glass coatings on chips might significantly increase the yield of assembled devices through visual inspections.

Another facet of glassing process investigation is the use of glass as a dielectric layer in connection with multilevel metalizat n required as the result of the growth in complexity of microcircuits.

Also, further investigation should be conducted to determine the optimum termination of glass in the bonding pad area for the flip-chip solder technique used with the batch attachment process on this program.

In the area of batch attachment, further investigation should consider the use of ultrasonic bonding in connection with the flip-chip approach. Also, the glassing technique developed on this program should be evaluated for compatibility with the beam lead type of attachment.

Further testing of glass coated microcircuits should be performed with the goal of determining a realistic quantitative failure rate. Also, since the incorporation of glassed chips in assemblies at the subsystem and system levels introduces a higher

level of reliability considerations, studies should be made of the actual reliability to be attained in various types of subsystem and system assemblies rather than following a practice of predicting the reliability levels by inference from the available data on the separate components used.

Since some form of coating material may be used over glassed chips for mechanical protection, tests should be conducted to investigate the effect on moisture resistance of variations in the coating process. For example, in the case of epoxy resin, the hardness, mix ratio, and effect of delay between mixing and use should be evaluated.

Related to the reliability of glassed chips, and assemblies of which they are a part, is the procedure followed in testing of electrical parameters. There is an increasing need to determine the optimum approach to testing and the selection of test parameters which will provide the most useful results for assuring that a glassed chip will function properly when incorporated in a larger assembly.

APPENDIX

Detailed Analysis of Results of Module Testing

Performed by the Contractor's R & QC Department

DETAILED ANALYSIS OF RESULTS OF MODULE TESTING PERFORMED BY THE CONTRACTOR'S R & QC DEPARTMENT

INTRODUCTION

In view of the relatively small quantity of devices utilized during this evaluation, it is more appropriate to utilize graphical displays of data than numerical statistics. The graphical displays present a correlation of individual initial parameter mesurements against the measurements made after 2000 hours for the 200° C storage and the 125° C 4 V reverse bias tests, and after moisture resistance testing for the environmental sequence. The correlation plots permit

a. evaluation of the parameter change experienced by individual devices,

b. indication of parameter frequency distribution at two reading periods,

c. a direct comparison of the different fabrication procedures, since the sample size permitted the data from all fabrication processes to be plotted on the same graph.

Because a total of twenty-six (26) parameters were measured on each device, only parameters selected to depict over-all device performance were plotted. These parameters are listed below.

Parameter	Conditions	Element
I_{CBO}	V_{CB} = 5 V	T_1
I_{EBO}	V_{EB} = 4 V	T_2
I_B	V_{CE} = 0.5 V, I_C = 50 μA	T_1
I_B	V_{CE} = 1 V, I_C = 1 mA	T_2
V_{CE}	I_C = 0.5 mA, I_B = 0.05 mA	T_1
V_{BE}	I_C = 50 μA, I_B = 10 μA	T_2
R	1 mA	R_1*
R	10 mA	R_4

The correlation plots are given in Figures 1 through 24. A discussion of the data follows.

DISCUSSION

I_{CBO} at 5 V, T_1

Environmental (Figure 1)

After moisture resistance there is a general increase in the leakage levels for both glassed and unglassed flip-chip devices; the unglassed devices have the larger increases. TO-5 enclosed devices remain stable. The initial distributions show a tight grouping at low leakage levels for TO-5 enclosed devices and higher initial values for flip-chip devices, with the unglassed devices exhibiting the highest initial leakage values. The changes in leakage current are attributed to the presence of moisture in the epoxy cap, and on the device surface.

*This parameter was read at 10 mA initially; the test condition was subsequently changed to 1 mA to decrease the test voltage and the associated power dissipation.

200°C Storage (Figure 2)

The general trend is for the glassed flip-chip devices to show a slight increase and the TO-5 enclosed devices to show a general decrease in value. The changes, however, are of rather small absolute values.

4 V Back Bias at 125°C (Figure 3)

No significant shifts were observed for any construction. Initial distributions, however, indicate that TO-5 enclosed devices exhibit the lowest leakage currents, and unglassed flip-chip devices the highest.

I_{EBO} at 4 V, T_2

Environmental (Figure 4)

After moisture resistance there was a tendency for the values of the glassed and unglassed flip-chips to increase. The TO-5 enclosed devices remained stable. The distributions indicate that the TO-5 enclosed devices have lower I_{EBO} than the glassed flip-chip devices, and the glassed flip-chip devices have generally lower I_{EBO} than the unglassed flip-chips.

200°C Storage (Figure 5)

There is no appreciable shift in the I_{EBO} measurement after 2000 hours. The TO-5 enclosed devices exhibit lower currents than the glassed flip-chips.

4 V Back Bias at 125°C (Figure 6)

There is no general shift in the I_{EBO} measurements after 2000 hours. The initial distributions overlap somewhat, but the

distribution for TO-5 enclosed devices is tighter and generally of lower value than for the flip-chip devices.

I_B at V_{CE} = 0.5 V and I_C = 50 μA

Environmental (Figure 7)

With the exception of those devices which were catastrophic failures, the stability of the devices is good. All of the catastrophic failures were flip-chip devices. The distribution of the TO-5 enclosed devices is tighter than that of the flip-chip distributions.

200°C Storage (Figure 8)

Four TO-5 enclosed devices showed a substantial improvement in h_{FE} after 2000 hours. The remainder of the devices, both TO-5 and flip-chip, showed good stability. The TO-5 devices exhibited a tighter distribution than did the flip-chip devices.

4 V Back Bias at 125°C (Figure 9)

The TO-5 enclosed devices showed a tight stable distribution after 2000 hours. There was a slight decrease in I_B after 2000 hours for the flip-chip devices, with the unglassed devices showing a slightly larger change than the glassed devices.

I_B at V_{CE} = 1 V and I_C = 1 mA

Environmental (Figure 10)

With the exception of the flip-chip catastrophic failures, the parameters are stable. The TO-5 enclosed devices have a tighter distribution than do the flip-chip devices.

200°C Storage (Figure 11)

Both the TO-5 enclosed and flip-chip devices show good parameter stability.

4 V Back Bias at 125°C (Figure 12)

Both the TO-5 enclosed and flip-chip devices show good parameter stability.

V_{CE} at I_C = 0.5 mA and I_B = 0.05 mA

Environmental (Figure 13)

TO-5 enclosed devices remain stable; flip-chip devices which were not catastrophic failures show an increase in this parameter. The unglassed flip-chips exhibited several very high readings, and almost all were catastrophic failures.

200°C Storage (Figure 14)

Several flip-chip devices showed an increase in this parameter. The TO-5 enclosed devices were stable. The distributions for both the TO-5 and flip-chip devices were relatively tight but the TO-5 devices were grouped around lower V_{CE} values.

4 V Back Bias at 125°C (Figure 15)

Unglassed flip-chips showed considerable distribution spread and both positive and negative changes. The glassed flip-chips showed a tighter distribution and some increase in the parameter value. The TO-5 enclosed devices were tightly grouped and stable.

V_{BE} at I_C = 50 μA and I_B = 10 μA

Environmental (Figure 16)

All devices that were not catastrophic failures showed a decrease in this parameter. The distributions of TO-5 enclosed devices were tighter than the flip-chip distributions. All catastrophic failures were flip-chip devices.

200°C Storage (Figure 17)

Both TO-5 enclosed and flip-chip devices were stable with the exception of three (3) flip-chips which showed considerable negative shift.

4 V Back Bias at 125°C (Figure 18)

All devices show a negative shift.

R_1 at 1 mA

Environmental (Figure 19)

With the exception of flip-chip catastrophic failures, the measurements indicate good stability.

200°C Storage (Figure 20)

These devices show a decrease in resistor value which can be explained by the fact that the test condition was changed after the initial reading. There was one (1) catastrophic failure due to delamination of the printed circuit metalization.

4 V Back Bias at 125°C (Figure 21)

There were no significant changes for any devices.

R_4 at 10 mA

Environmental (Figure 22)

The glassed flip-chips and the TO-5 enclosed devices remained relatively stable, except for three (3) glassed flip-chips which became catastrophic. The unglassed flip-chips exhibit an increase in value. The distribution of the TO-5 enclosed devices was rather tight; the flip-chip distribution was spread.

200°C Storage (Figure 23)

The distribution of the TO-5 enclosed devices was tight and the measurements were stable. The distribution of the flip-chip devices was spread and devices indicated both positive and negative shifts.

4 V Back Bias at 125°C (Figure 24)

The distribution of the TO-5 enclosed devices was tight and stable. The distributions of the glassed and unglassed flip-chip devices were spread and showed shift, with the unglassed devices showing the larger shifts. Only certain devices which had been subjected to the environmental test sequence were subjected to a 4 V moisture resistance test with bias. (See Table II, page 35, of the body of the report.) The flip-chip devices exhibited a considerable number of failures during this test, but no TO-5 enclosed device failures were observed.

CONCLUSION

Because of the small quantity of test devices involved, no attempt has been made to establish a failure rate or reliability level for these particular devices. A comparison of the results obtained for the different fabrication processes can be made by reference to Tables III, IV and V (pages 37, 38 and 39, respectively) in the body of the report. Several generalizations based on a study of the test results are given below.

The devices assembled in TO-5 enclosures demonstrated good stability throughout all of the testing and, in general, all of the distributions were tight. The stability of both the glassed and unglassed flip-chip devices was satisfactory through the reverse bias and 200° C storage testing, but these devices did not exhibit the same degree of stability and tightness of distribution as did the TO-5 enclosed devices.

The flip-chip devices subjected to the environmental sequence passed thermal shock, mechanical shock, vibration and centrifuge testing without any significant change in parameter values, but suffered a considerable amount of catastrophic failures during moisture resistance and moisture resistance with bias testing. The analysis of the failed devices from these tests indicated that the mechanism was electrolytic corrosion of the interconnecting metalization caused by the introduction of moisture and the subsequent application of voltage, either during the test itself or during the measurement of electrical parameters.

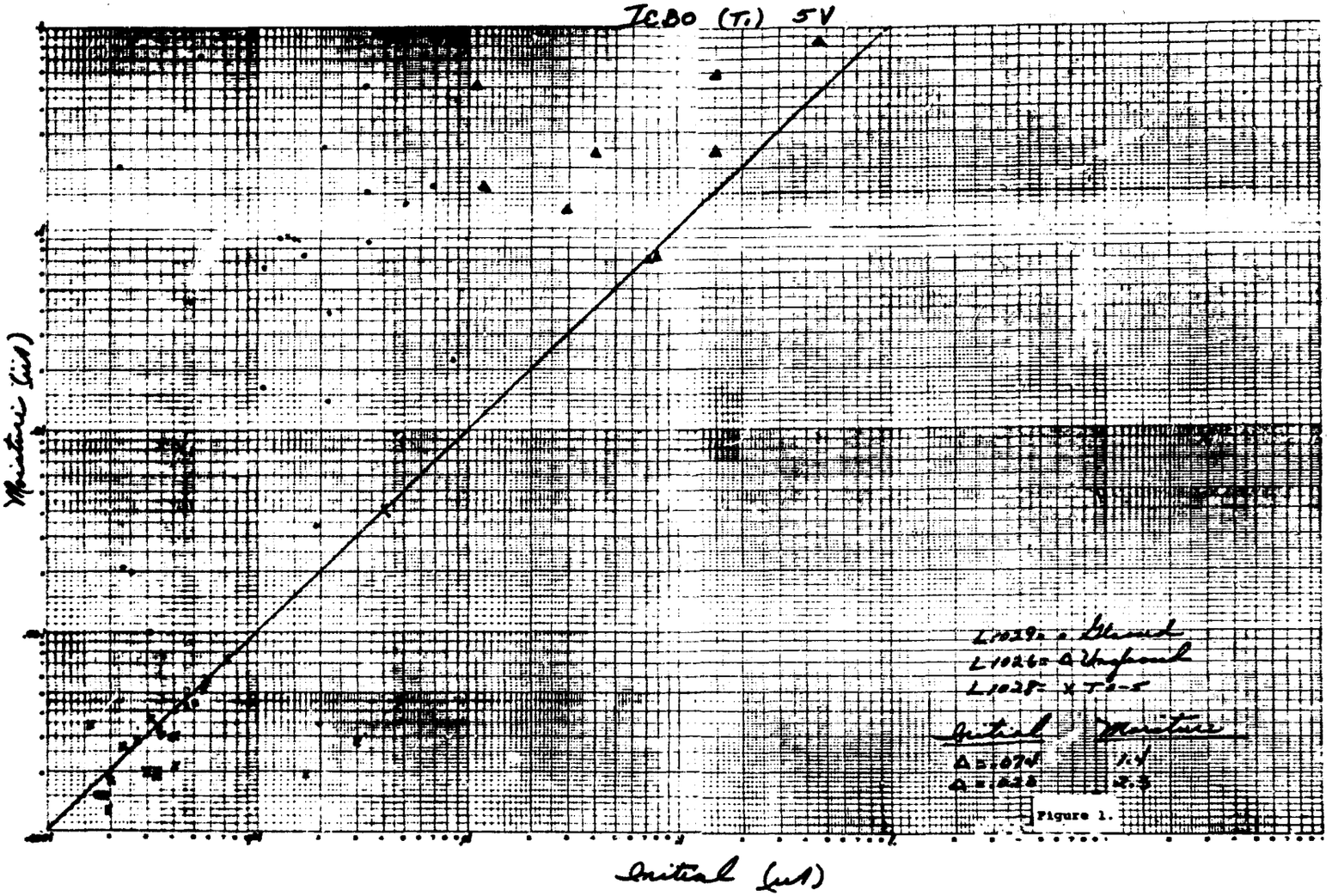

IC.BO (T.) 5V
Moisture (wt)
Initial (wt)
L1029 = Blend
L1026 = Unblend
L1025 = T2-5
Initial
Moisture
Δ 5.07%
1.4
Δ = .025
2.5

Figure 1.

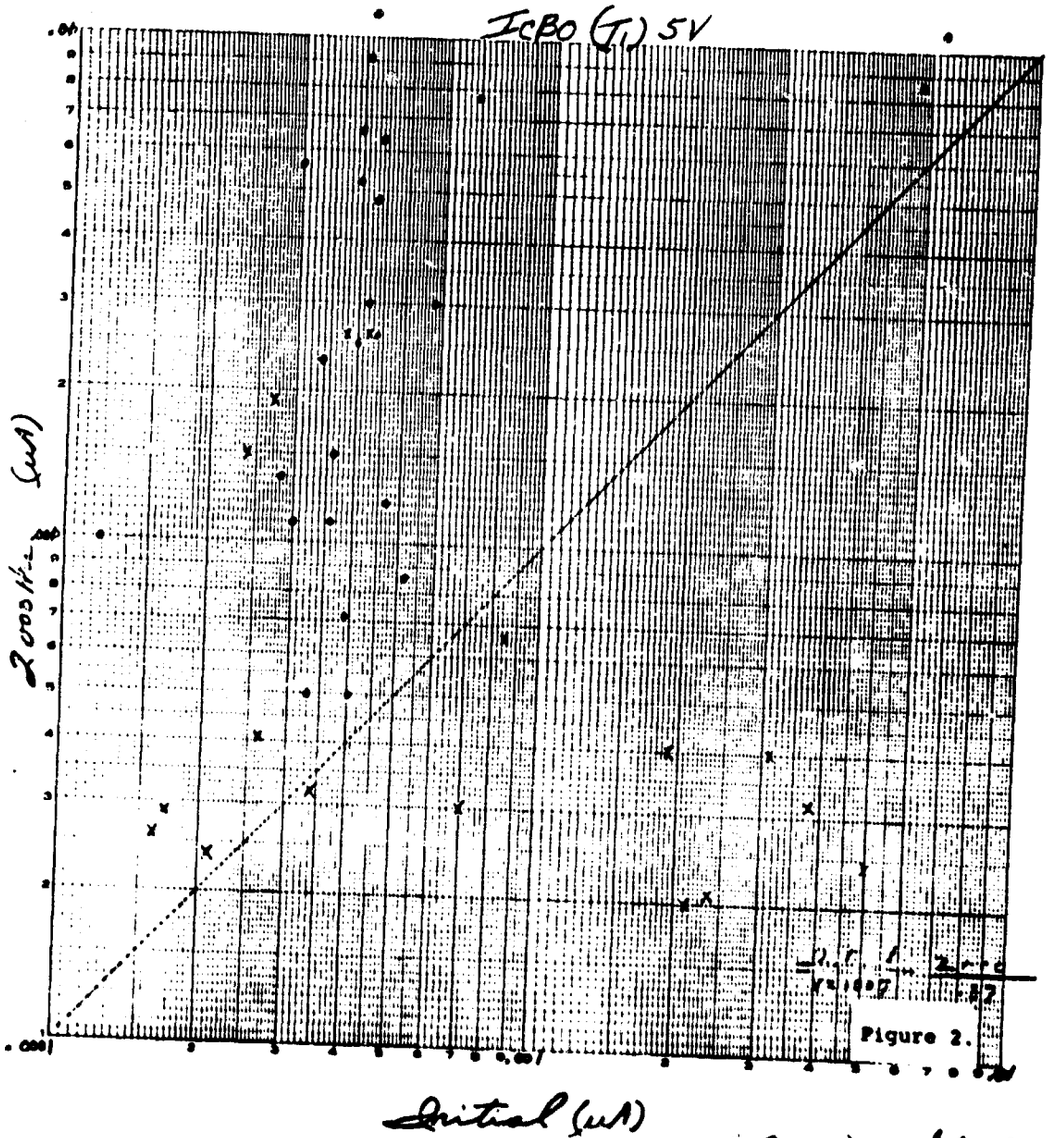


Figure 2.

L 2052 } = • Glued
L 2053 }

L 2054 = X TO-5

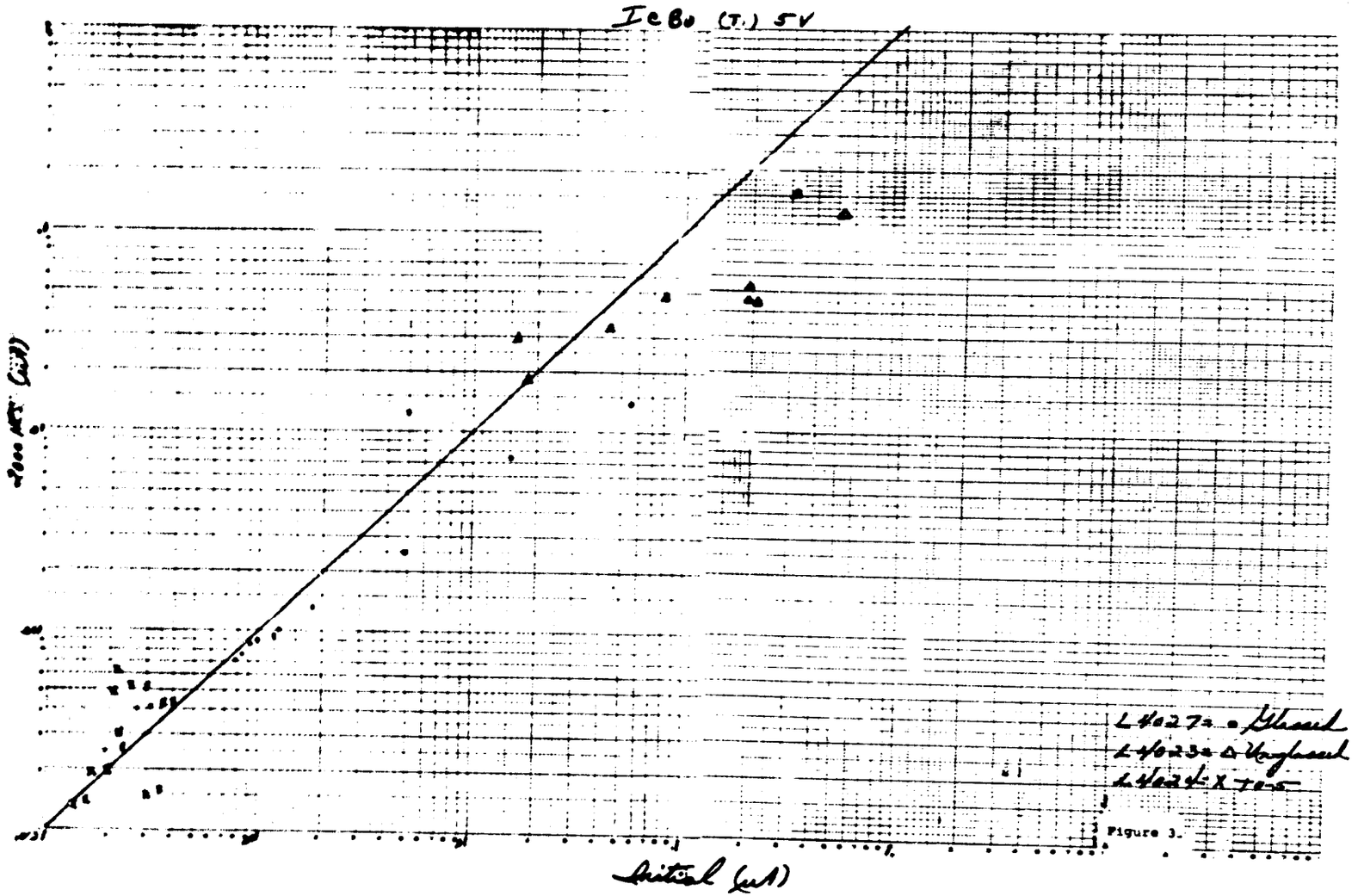

I_{CBO} (T.) 5V
2000 Hrs (Hill)
Initial (μA)
L40271 ● Ground
L40232 △ Unground
L40234 X Tons

Figure 3.

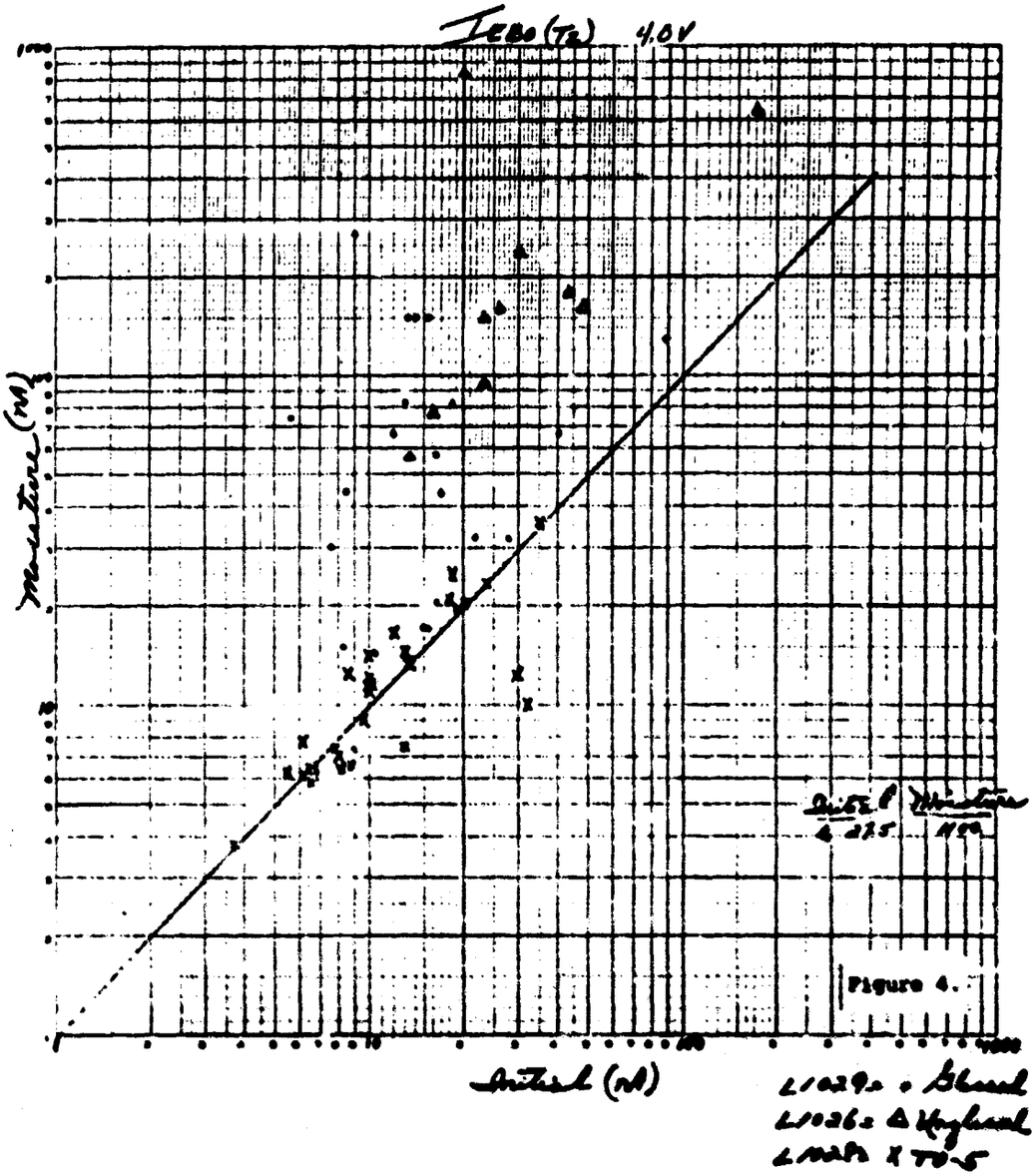


Figure 4.

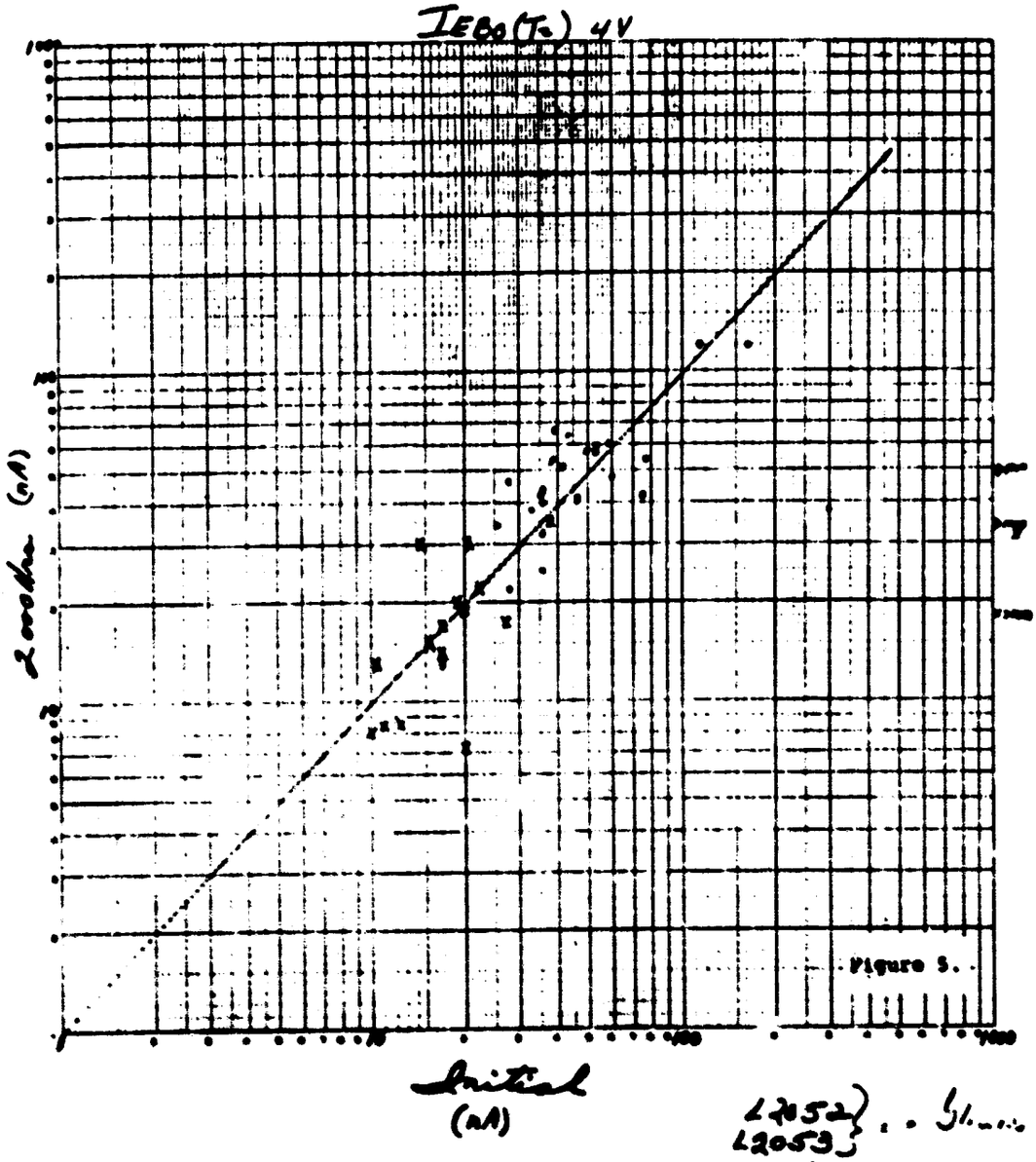
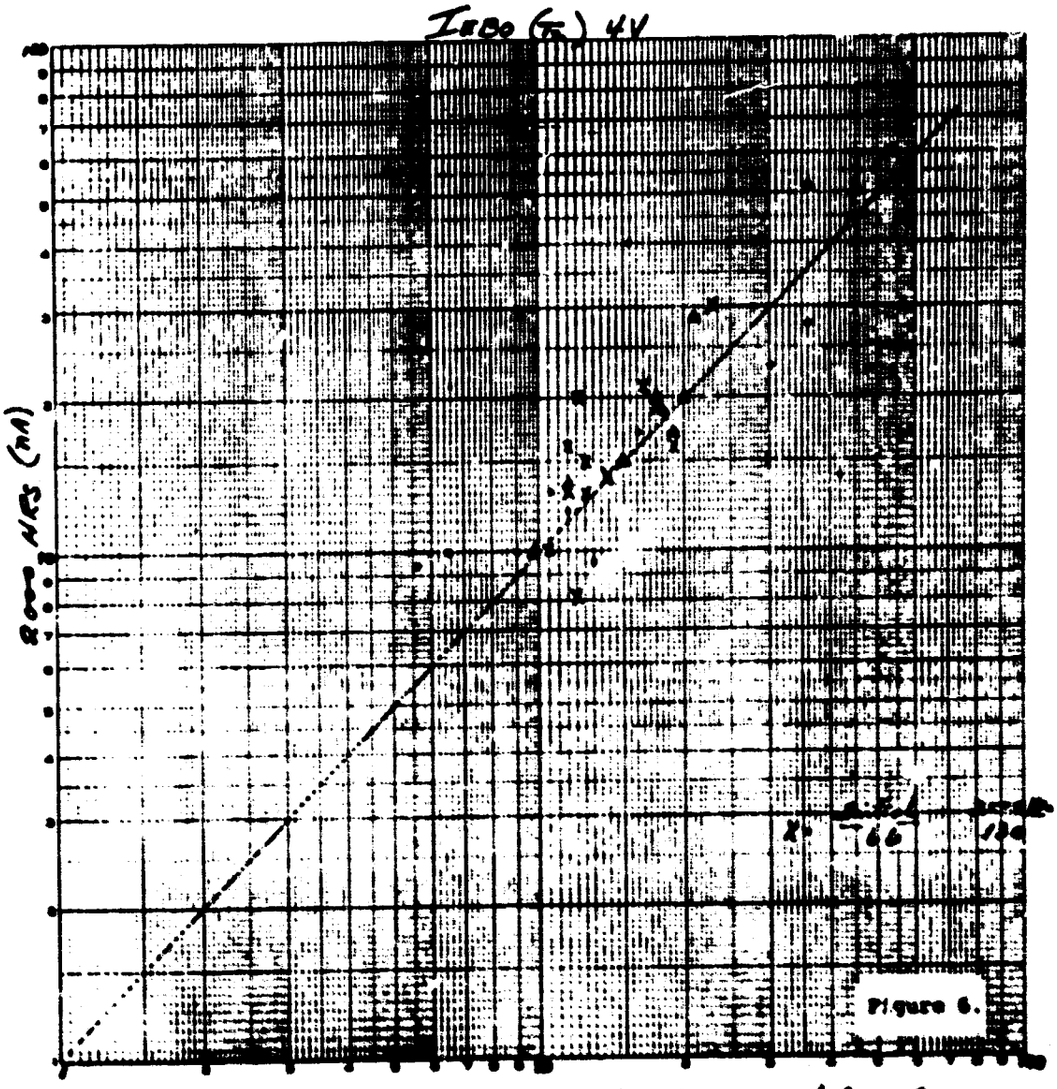


Figure 5.

L2052
L2053 } . . 5V . . . .

L2054 = 1 TO 5


I_{SDO} (Fe) 4V
Initial (nA)
Figure 6.

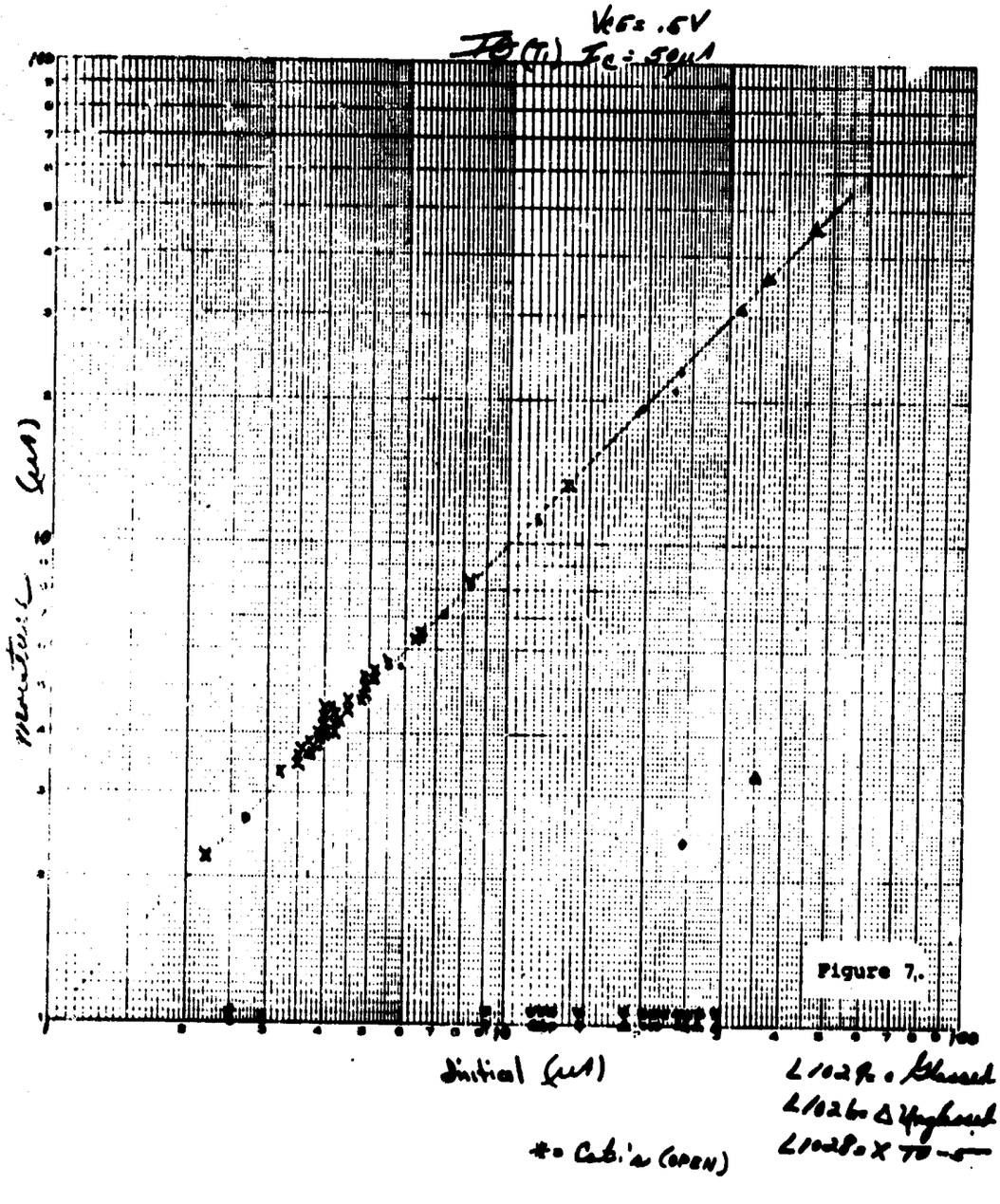
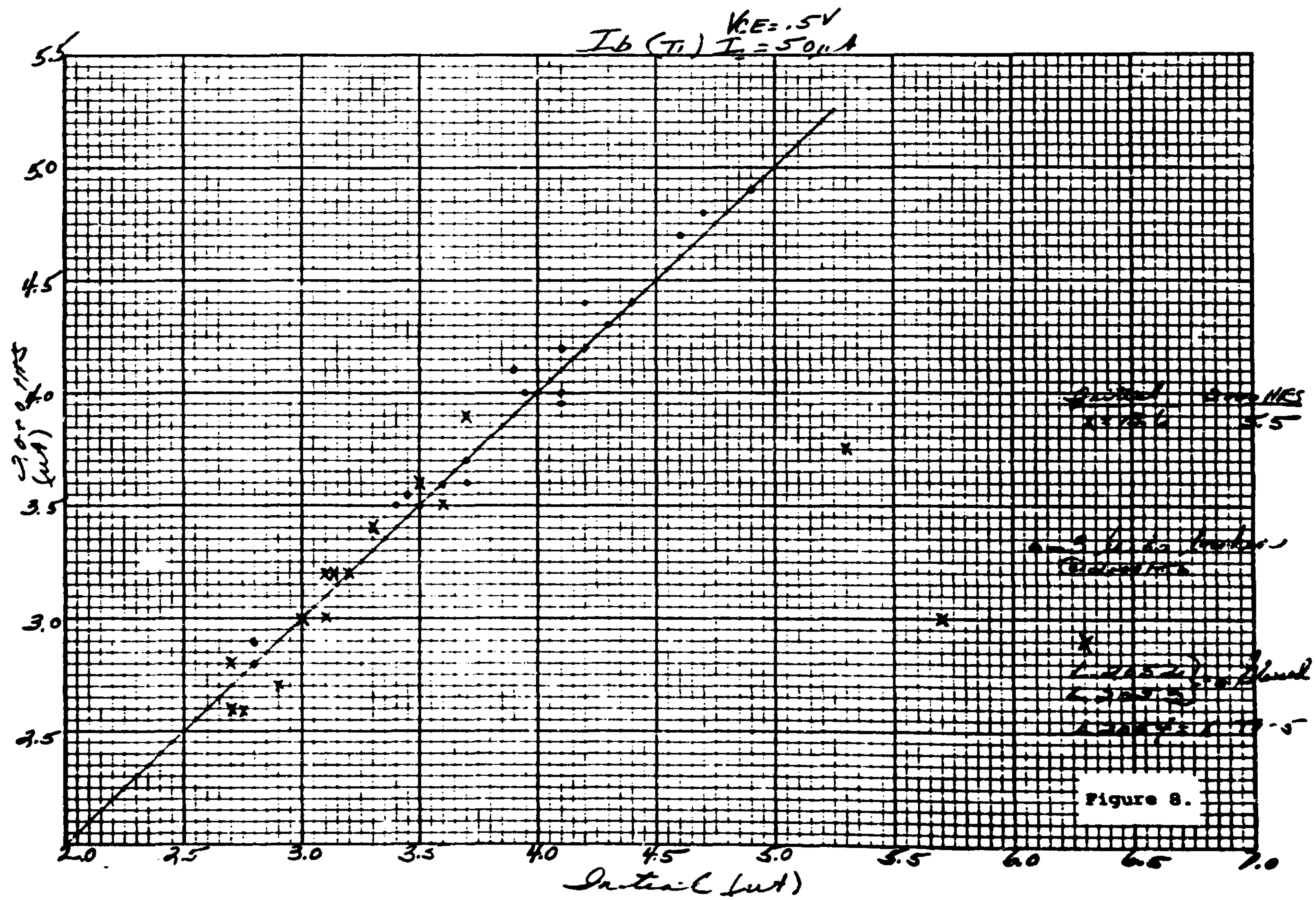

VGS = .6V
IB (μA) IC = 50μA
Initial (μA)
L1028 • Closed
L1026 △ Unplaced
L1028 X 70 —
* = Calc'd (OPEN)

Figure 7.


Ib (T1) VCE = .5V IC = 50μA
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
2.5
3.0
3.5
4.0
4.5
5.0
5.5
6.0
6.5
7.0
Initial (μA)
Figure 8.

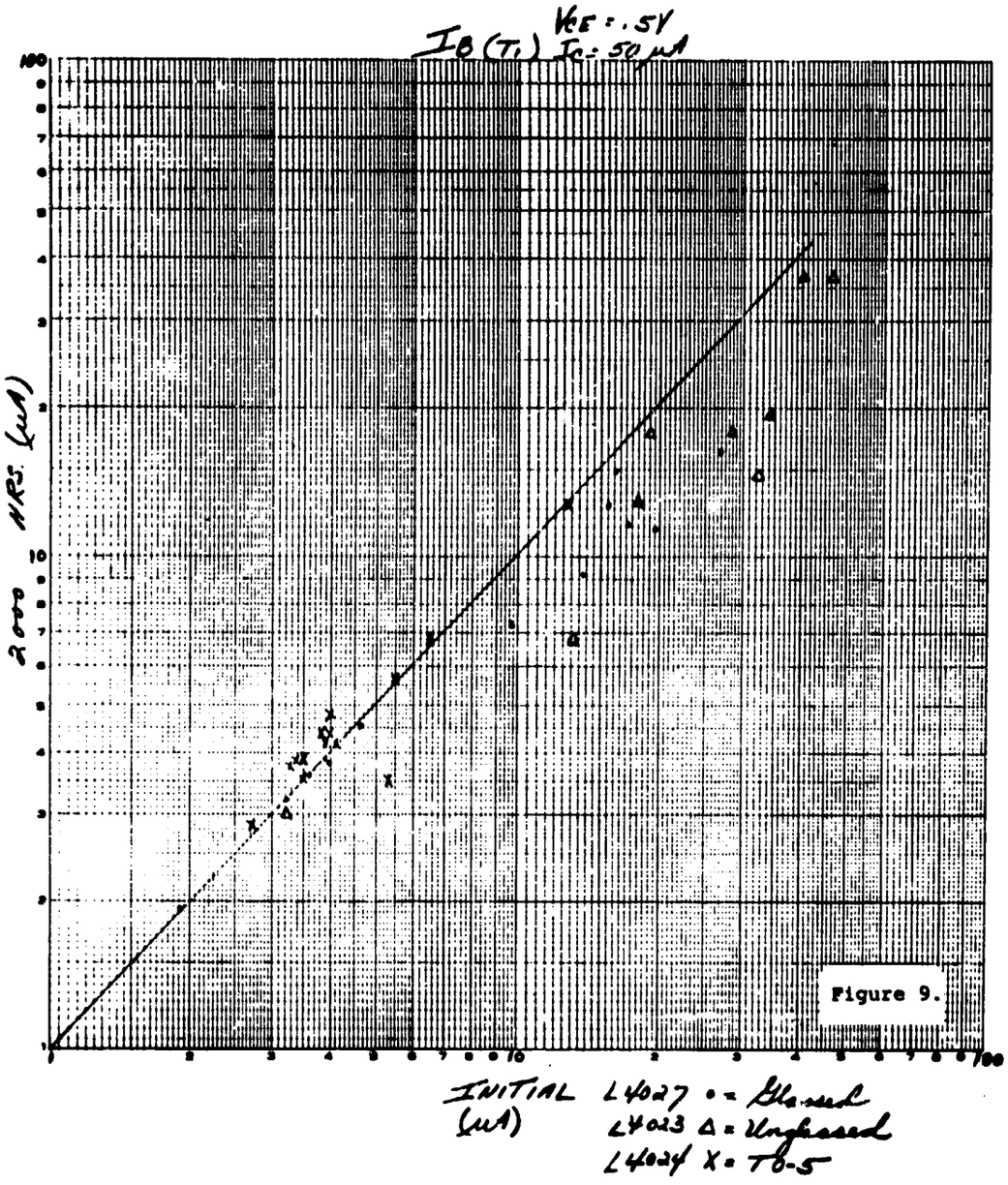

$I_B(T_1)$ V_{CE} = .5V
I_C = 50 μA
2000 HRS. (μA)
INITIAL (μA)
L4027 ○ = Glassed
L4023 Δ = Unglassed
L4024 X = TO-5

Figure 9.

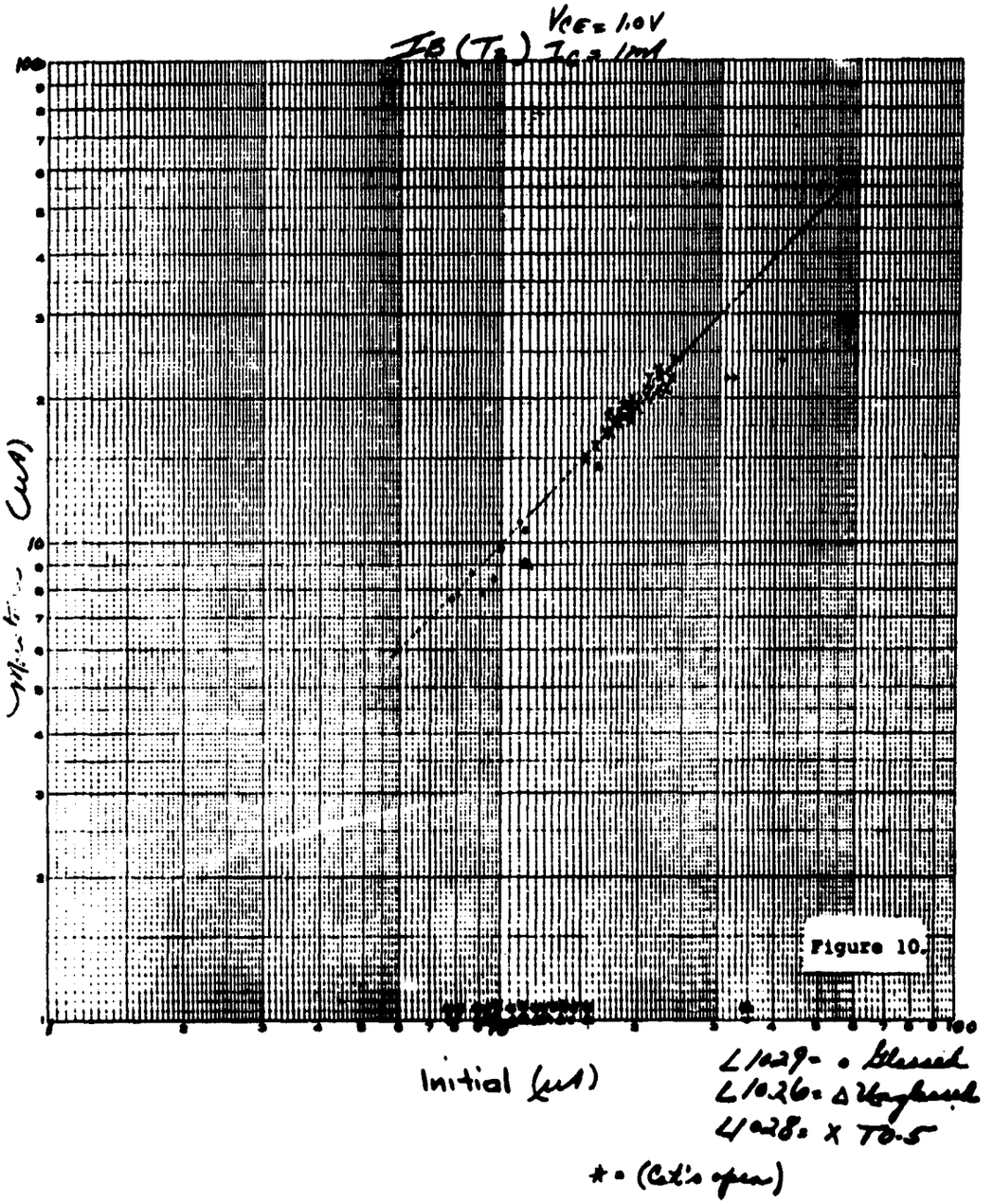

V_{CE} = 1.0V
$I_B(T_2)$ I_C = 1mA
Initial (μA)
∠1029 - ○ Blessed
∠1026 - △ Unpackaged
∠028 - × TO-5
★ - (Cal's open)

Figure 10.

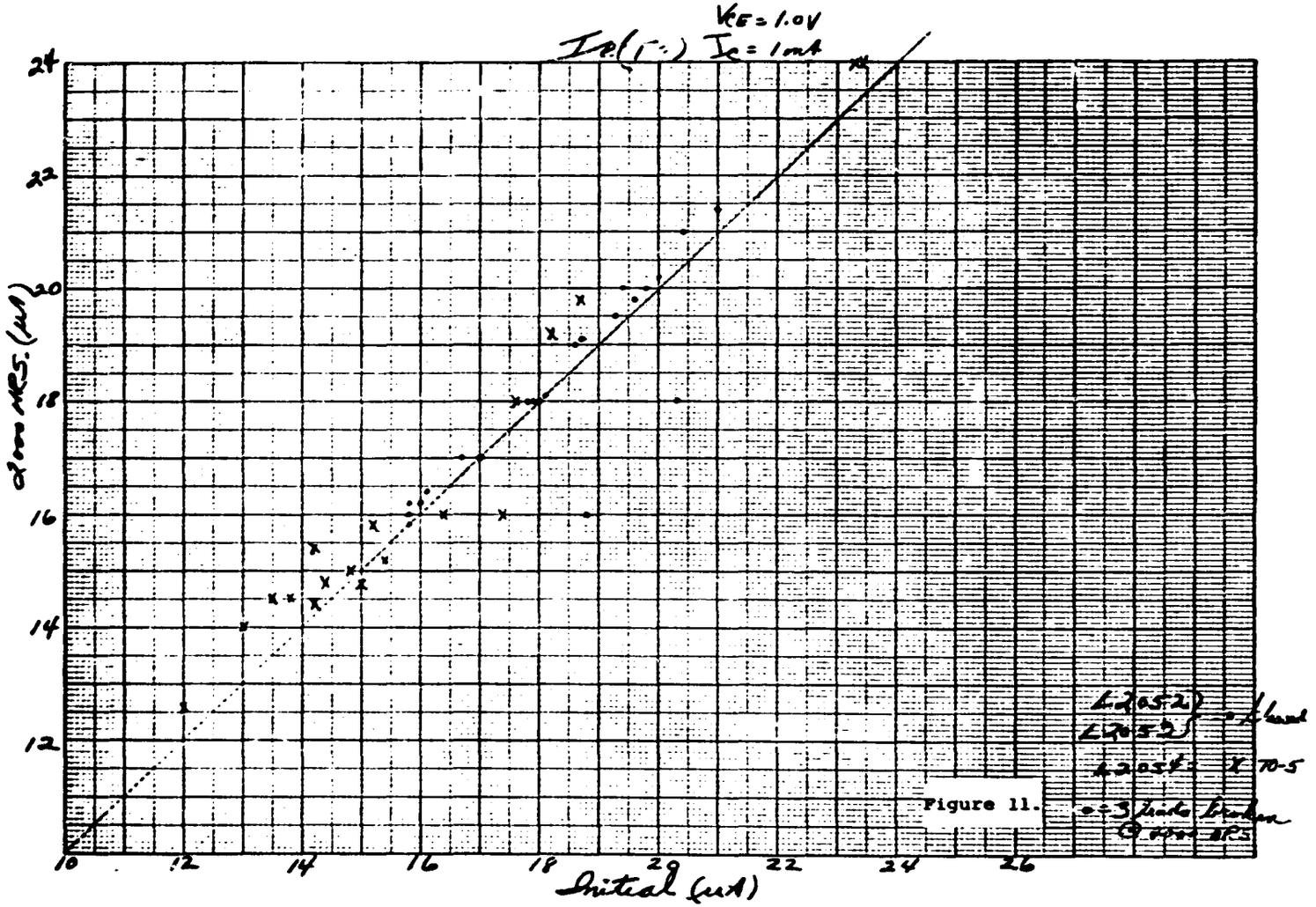

V_{CE} = 1.0V
I_B (μA) I_C = 1mA
24
22
20
18
16
14
12
10
12
14
16
18
20
22
24
26
Initial (μA)
Final MES. (μA)

Figure 11.

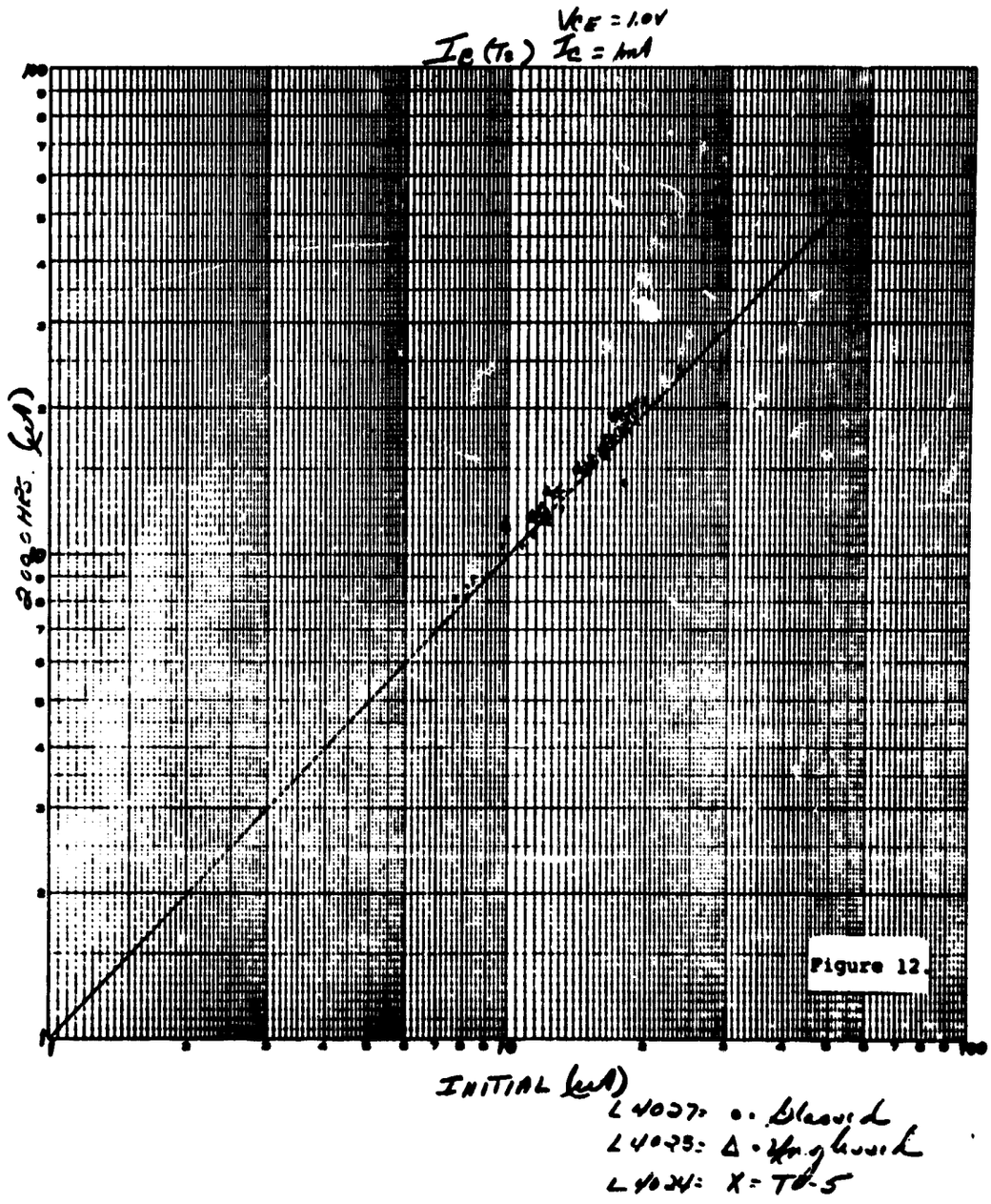

V_{CE} = 1.0V
I_B (T_0) I_C = 1mA
INITIAL (μA)
L4037: ○ Blessil
L4023: Δ · Hughes L
L4034: X = TO-5

Figure 12.

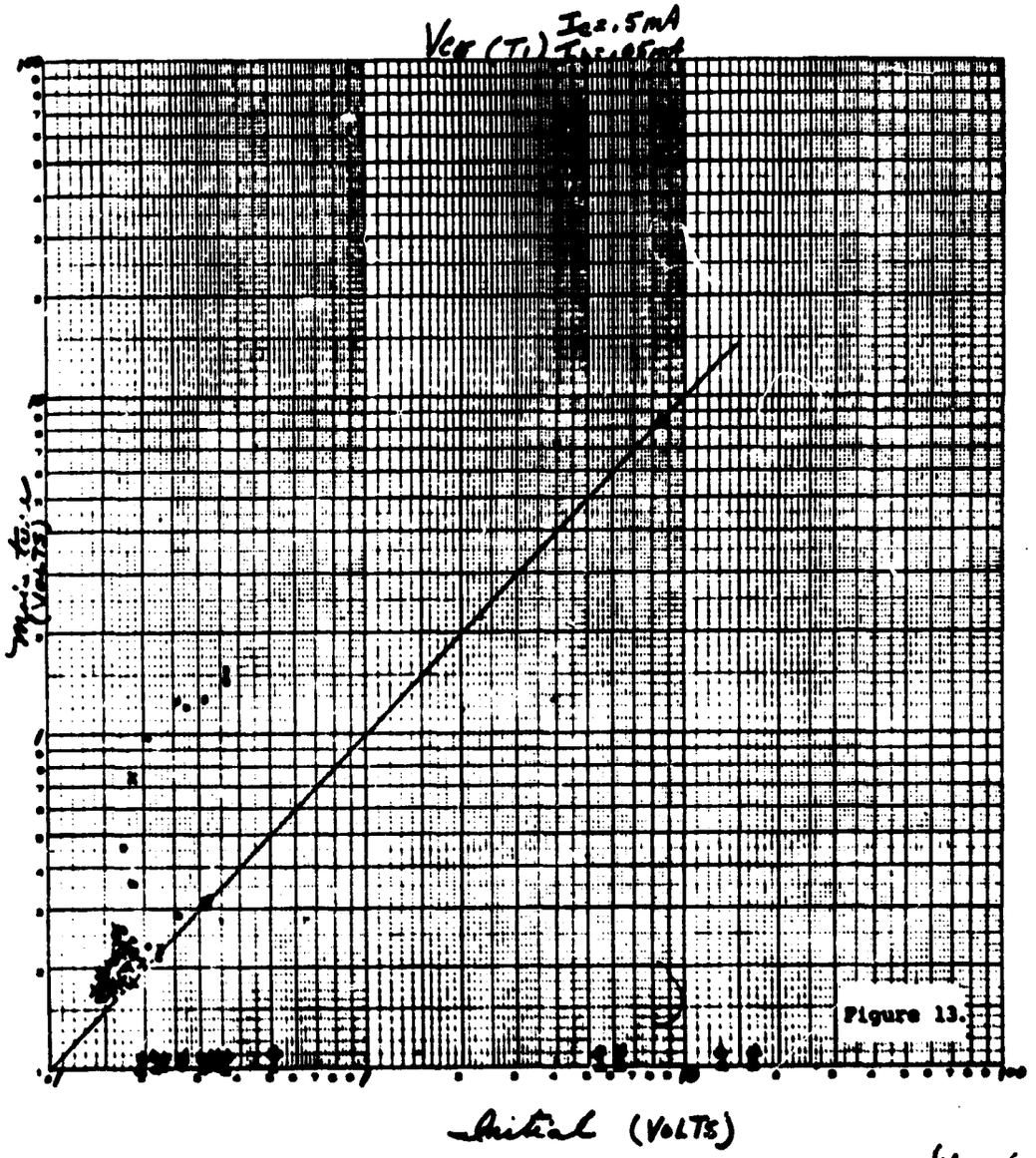


Figure 13.

∠1029 = ○ Blanch
∠1026 = △ Highland
∠1028 = × Tolo

* Cal'd (open)

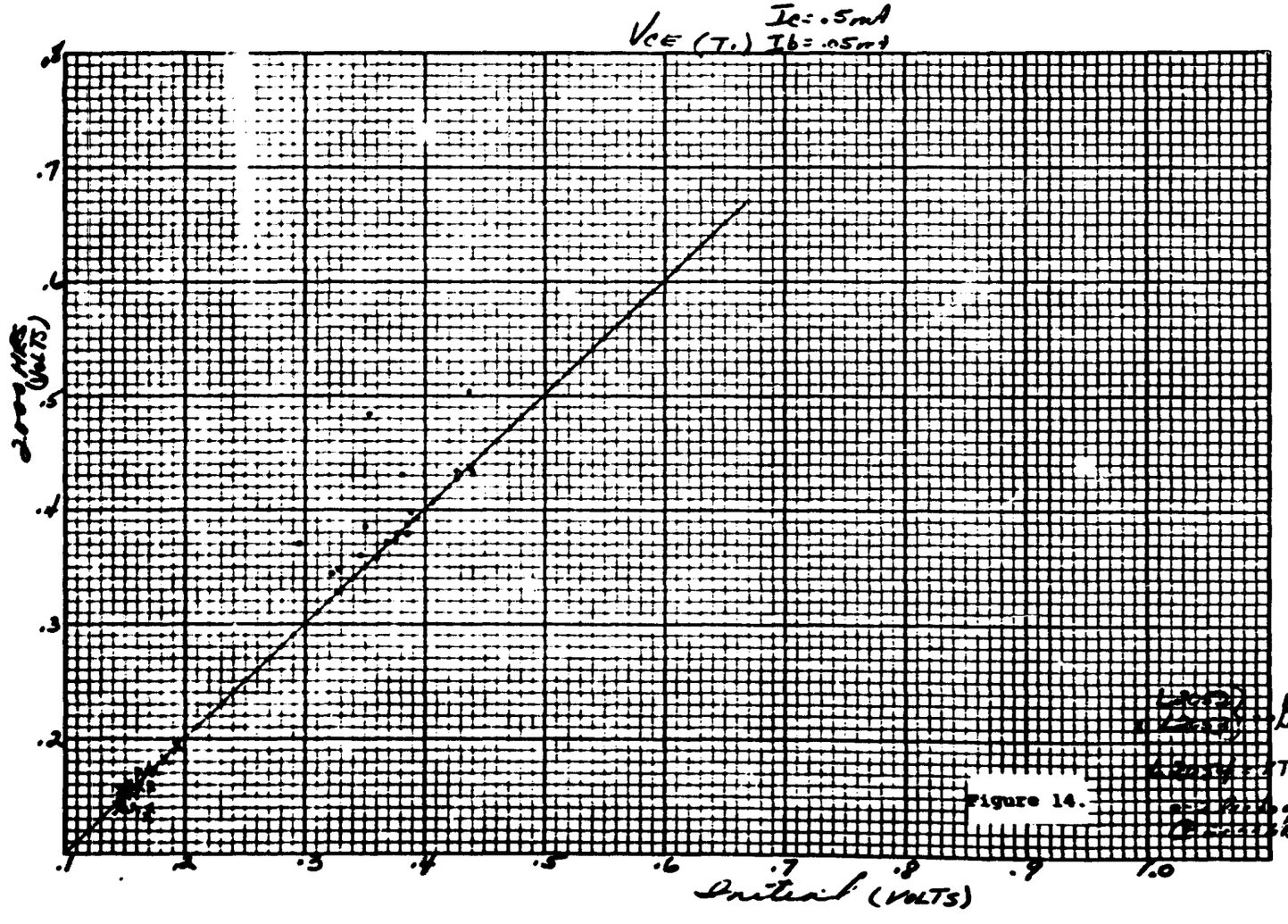


Figure 14.

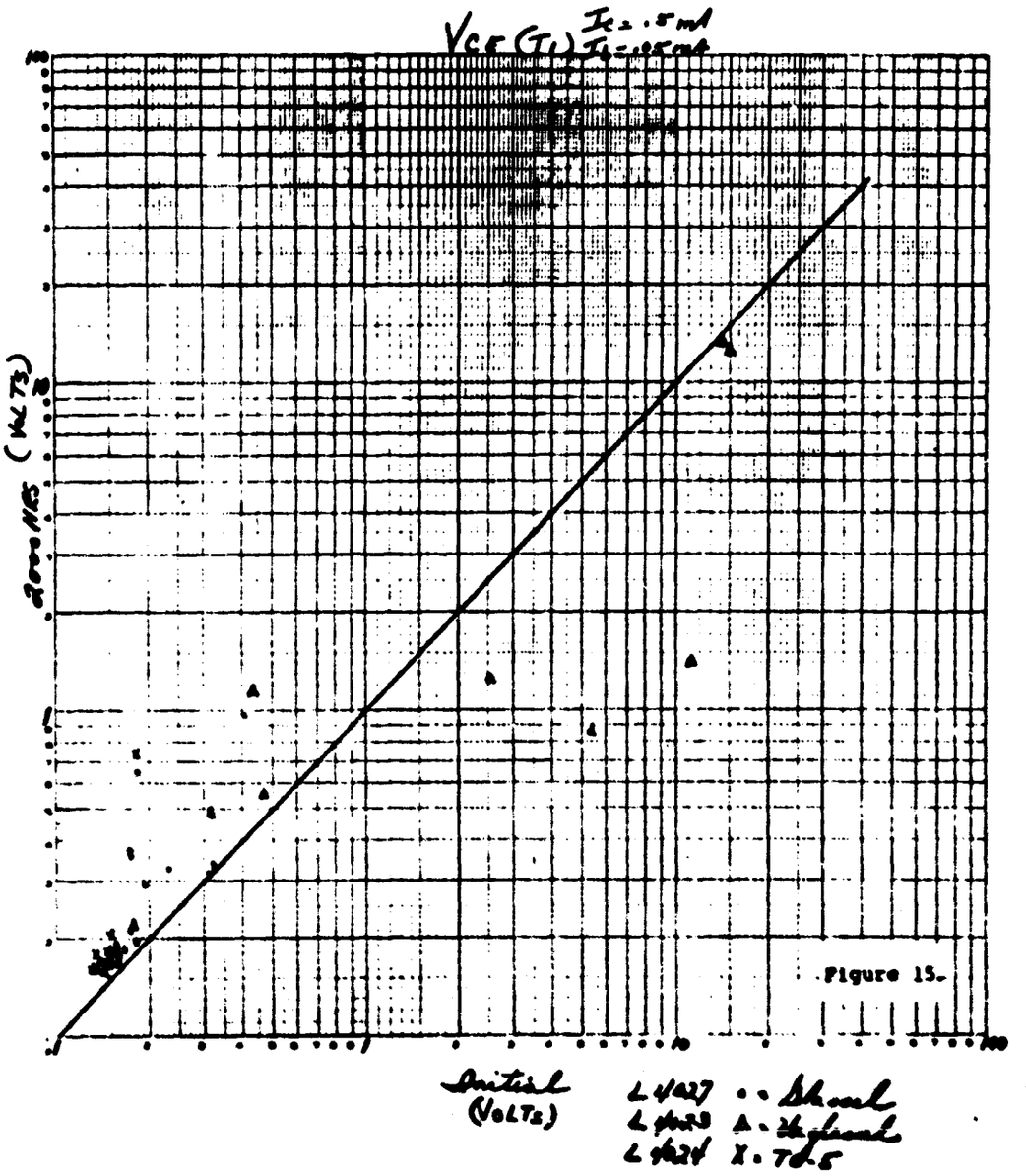
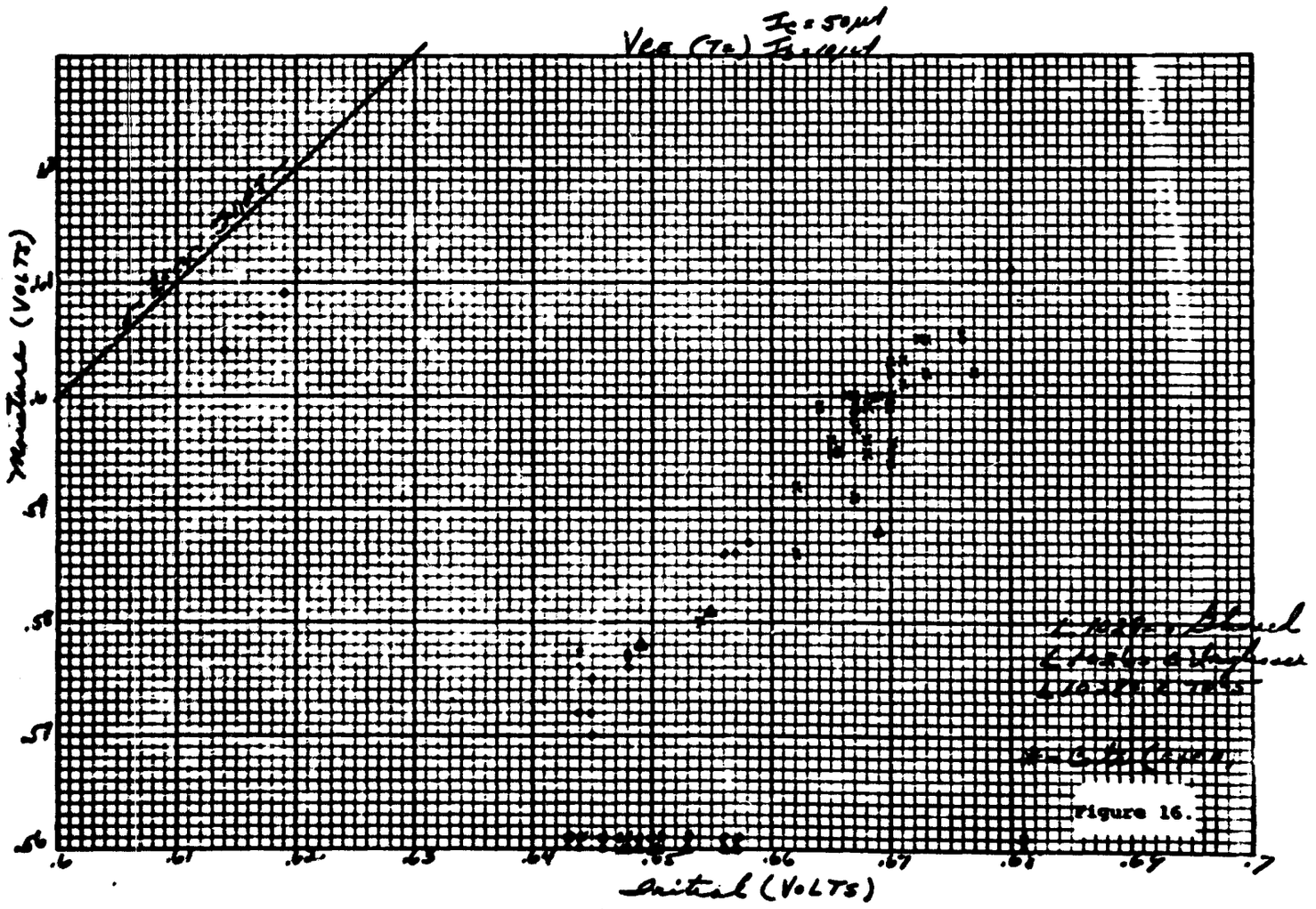


Figure 15.



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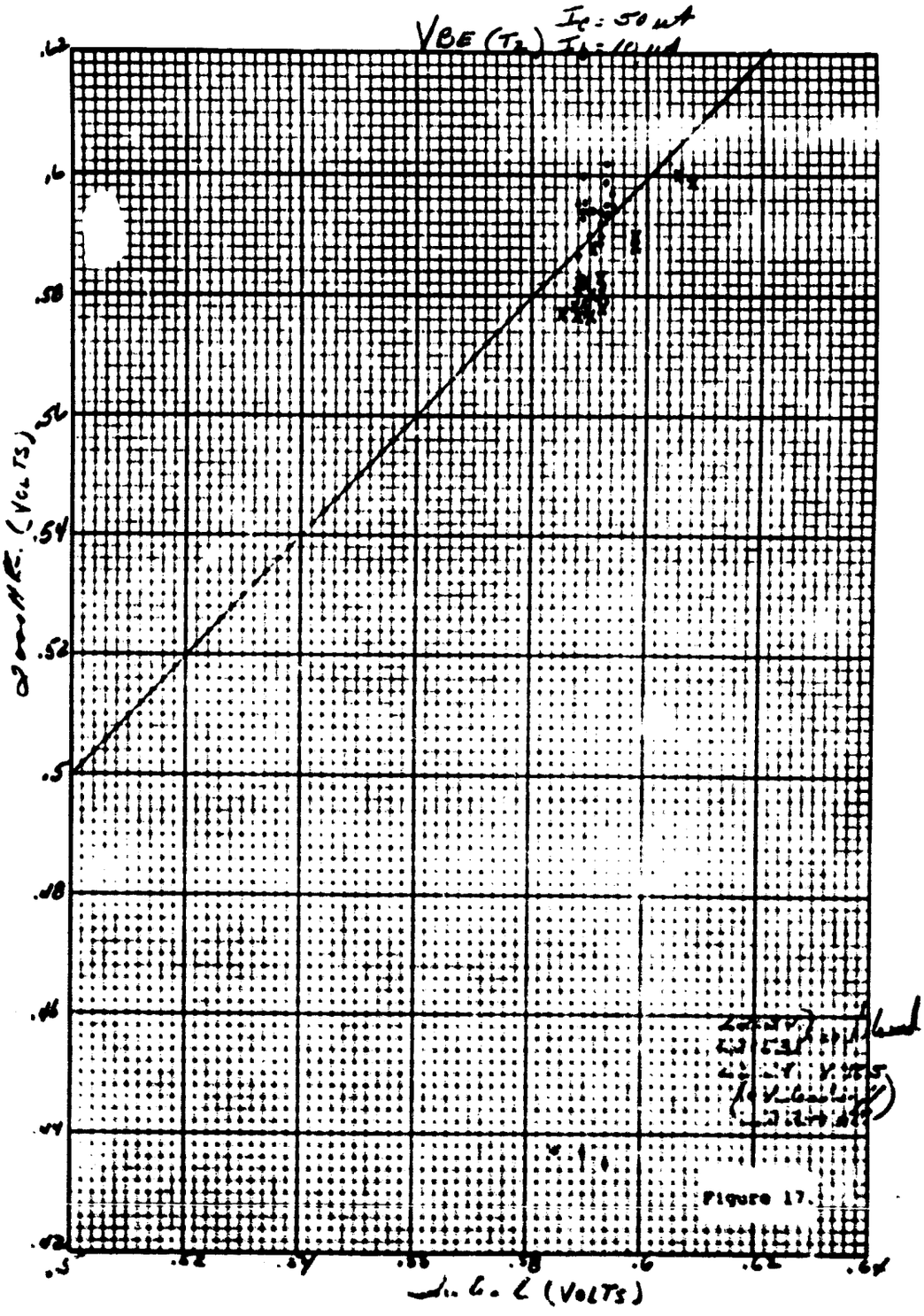

Figure 17.

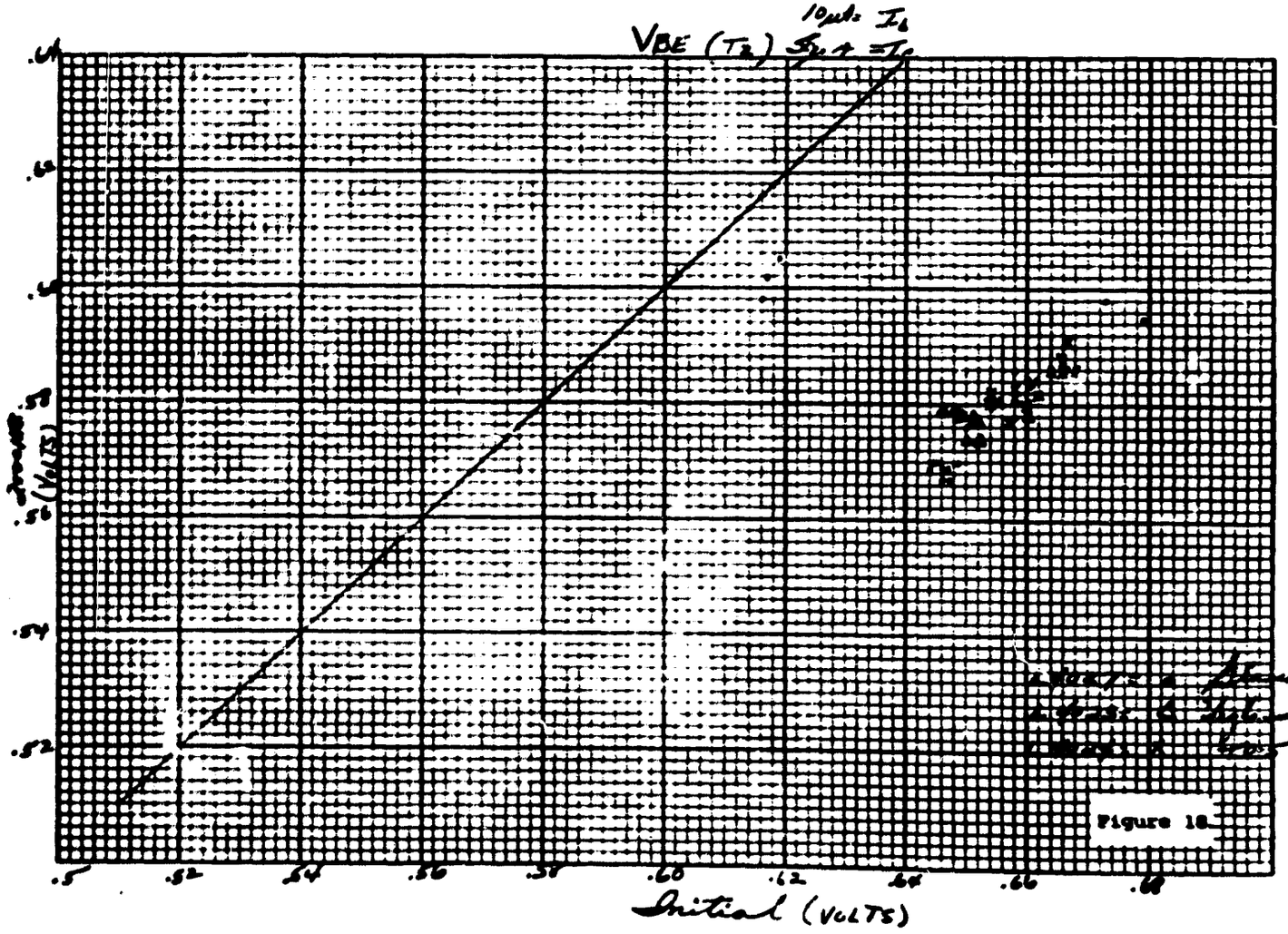

Figure 18

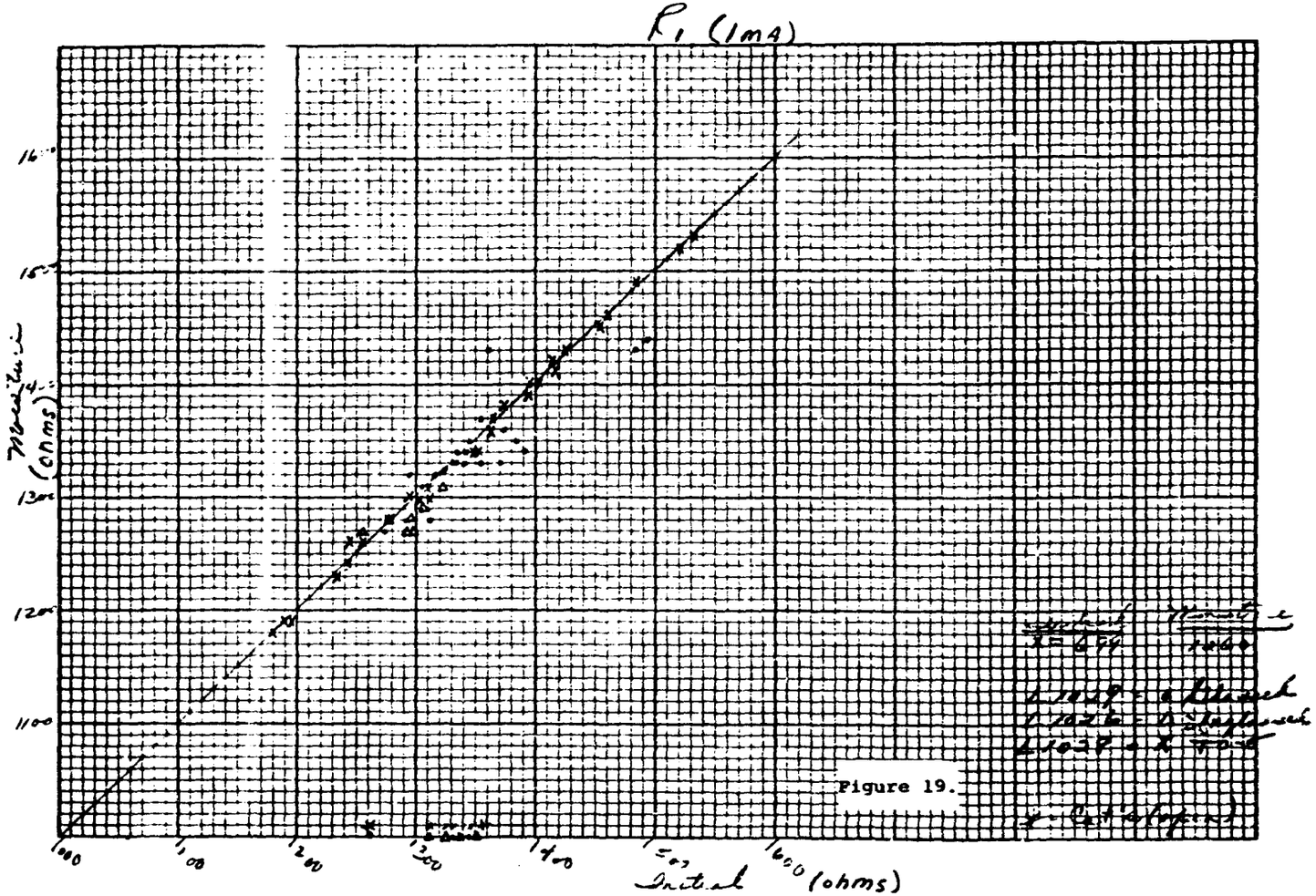
R_1 (1mA)
1600
1500
1400
1300
1200
1100
Millivoltmeter (ohms)
1000
1100
1200
1300
1400
1500
1600
Initial (ohms)

Figure 19.

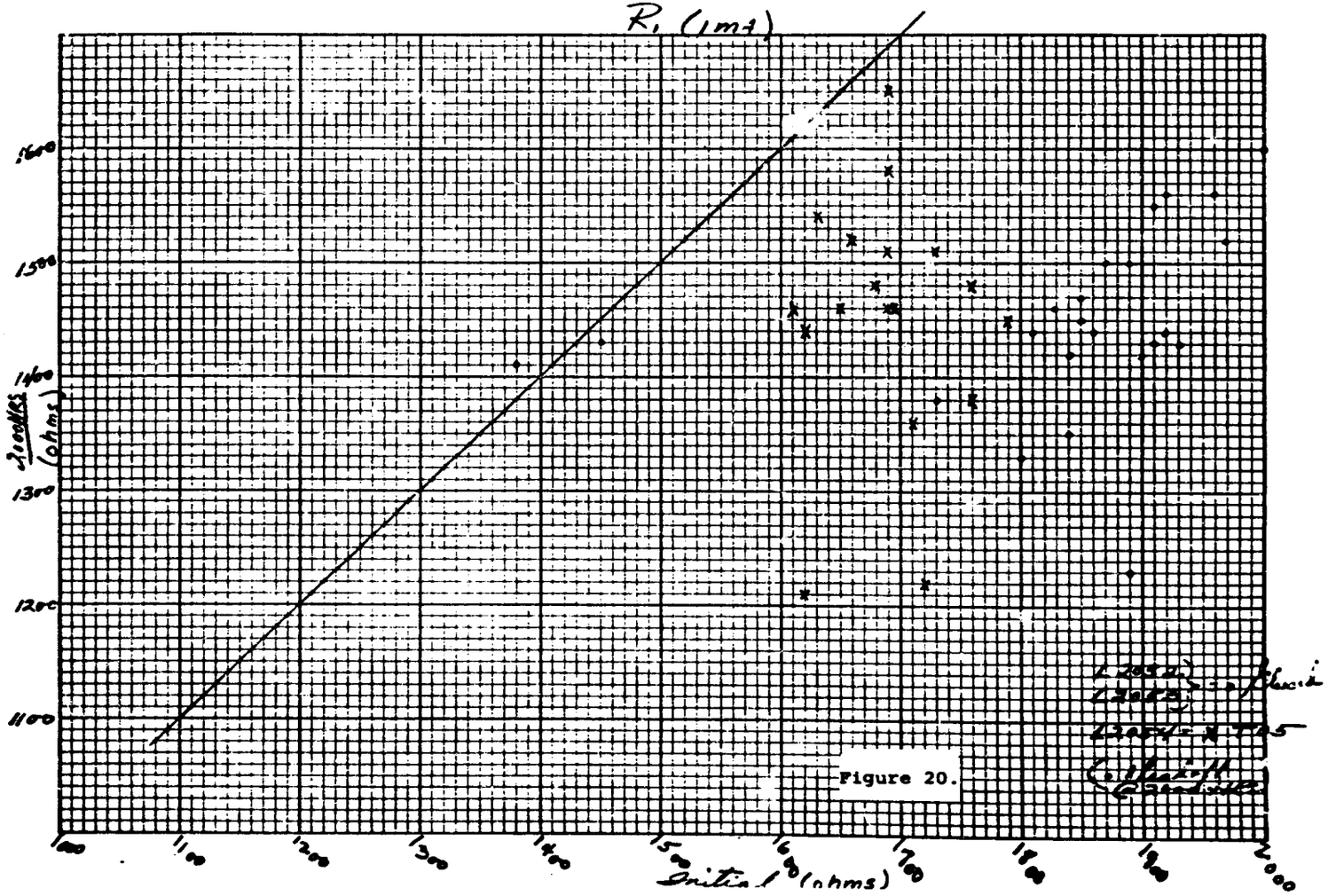
R, (1m4)
1600
1500
1400
1300
1200
1100
2nd RS (ohms)
1100
1200
1300
1400
1500
1600
1700
1800
1900
2000
Initial (ohms)

Figure 20.

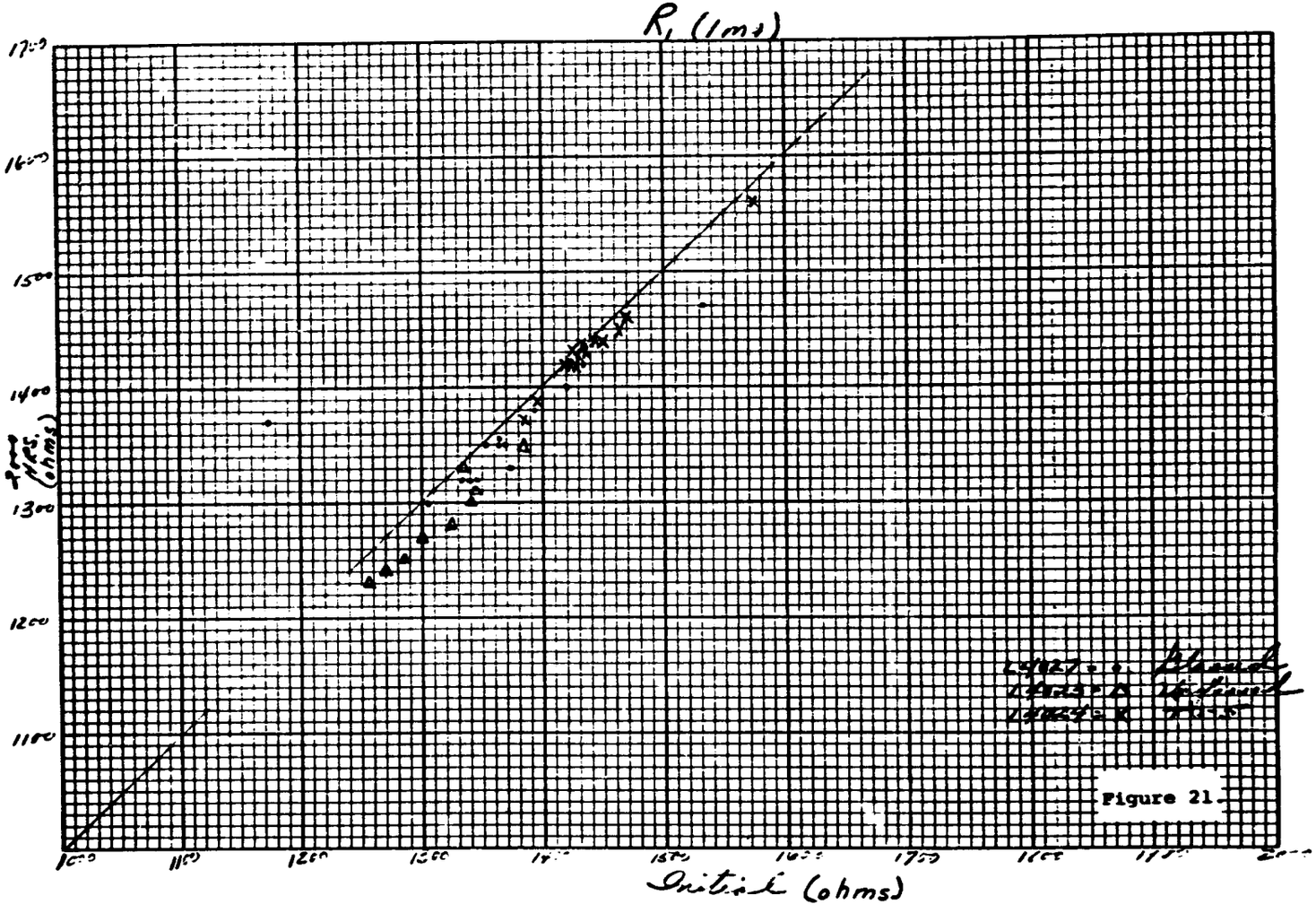
R, (1ms)
1700
1600
1500
1400
1300
1200
1100
1000
1100
1200
1300
1400
1500
1600
1700
1800
1900
2000
Initial (ohms)

Figure 21.

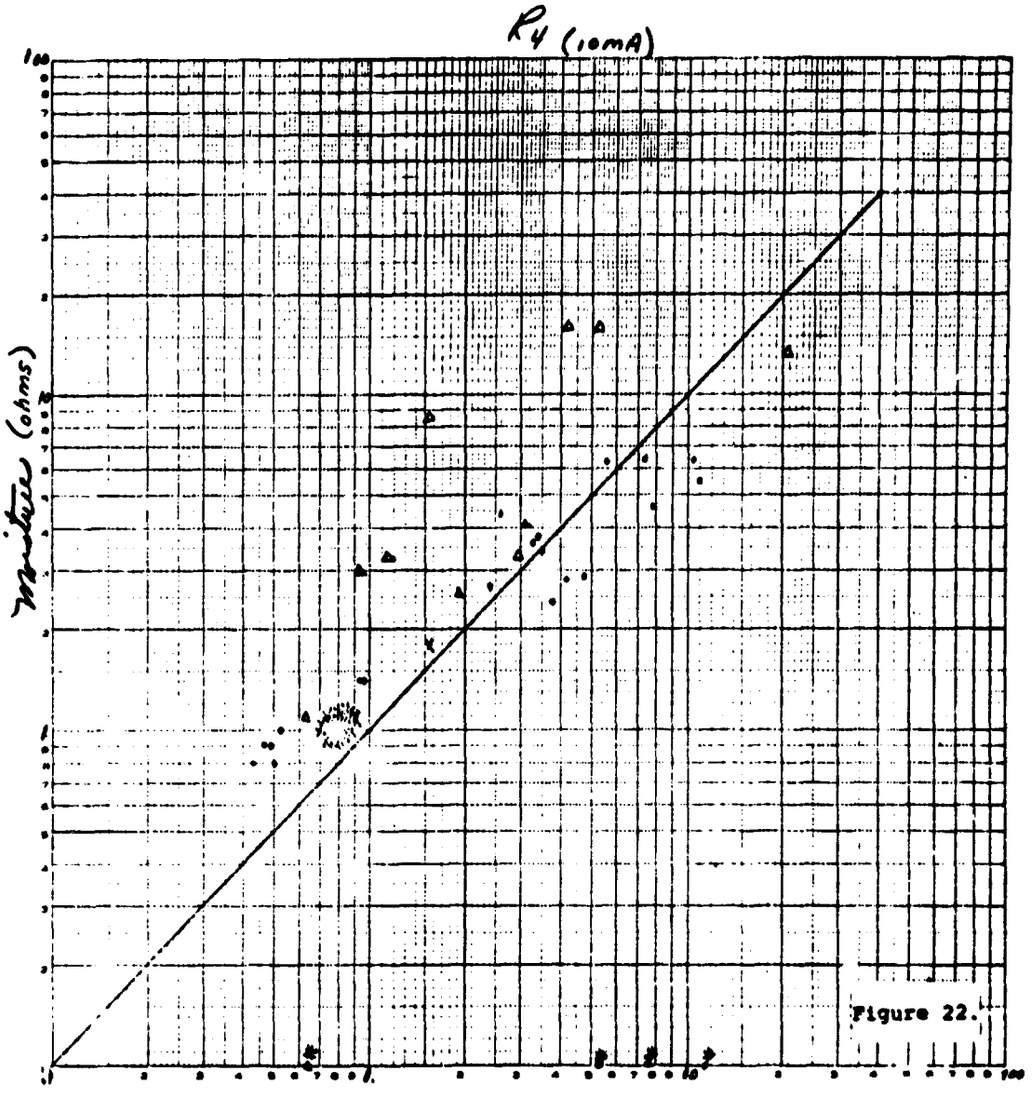
R_4 (10mA)
Minitec (ohms)
Initial (ohms)
L1029 = ○ Glass
L1026 = △ Hafnia
L1028 = X TRS
* = Cat'y. (p...)

Figure 22.

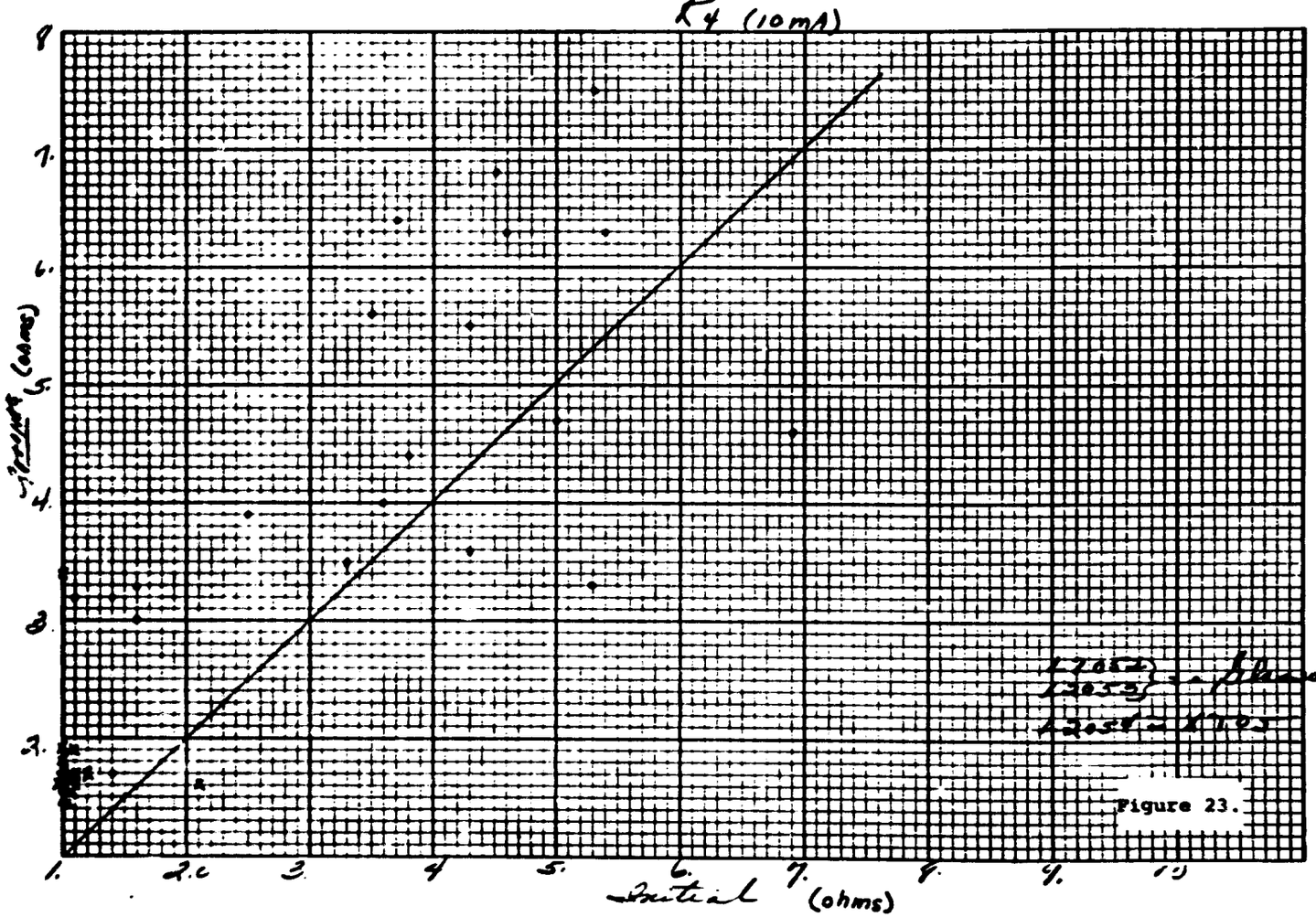

Figure 23.

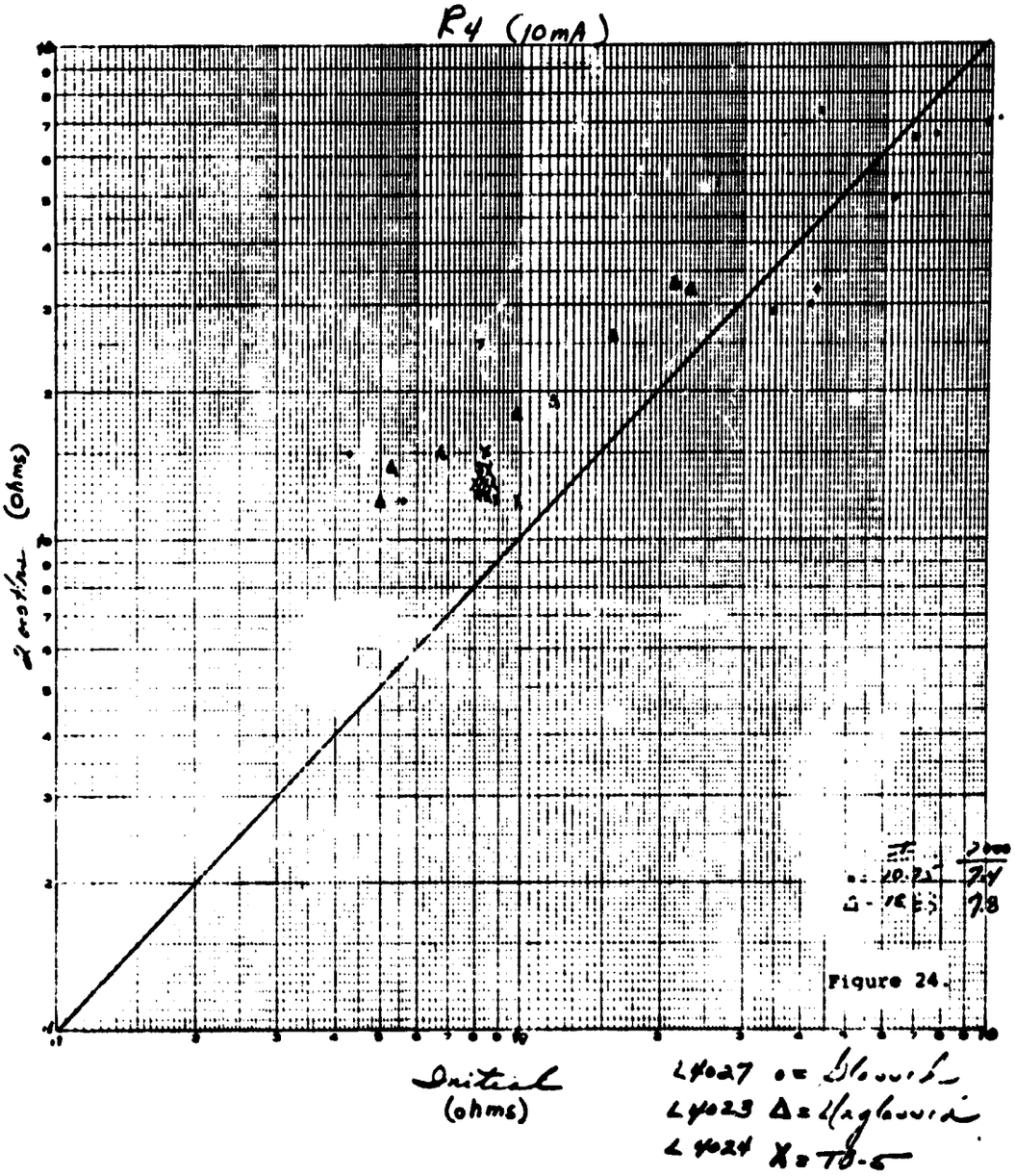

Figure 24.

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5 AUTHOR(S) (Last name, first name, initial)

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13 ABSTRACT

An over-all process was developed for glass coating of silicon integrated circuit chips and batch attaching them to an appropriately processed substrate. The techniques developed were demonstrated by delivery of four 10-chip arrays consisting of glassed silicon micro-circuits flip-chip assembled on a plug-in printed circuit board. Detailed information is provided concerning wafer glassing and other processing leading to flip-chip assembly.

In addition to the delivery of the final exploratory development models, other development units were fabricated and subjected to a test sequence intended to demonstrate the effectiveness of the developed process. Although the assignment of a quantitative failure rate was considered unrealistic because of the limited sample size, the analysis of the test data led to the conclusion that no catastrophic or major deleterious effects result from the combined glass and batch assembly process.

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Security Classification

14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
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Glass Passivation						
Vapor Plated Glass						
Face Down Solder Bonding						
Batch Assembly						
Epoxy Coating						

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